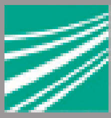


Fraunhofer

ISIT

FRAUNHOFER-INSTITUT FÜR SILIZIUMTECHNOLOGIE ISIT

Achievements and Results Annual Report 2009

Achievements and Results Annual Report

2009

Preface 6

Brief Portrait 12 Fraunhofer ISIT Research and Production at one Location

Main Fields of Activity 14 Microsystems Technology (MEMS) and IC Design

16 IC Technology and Power Electronics

18 Biotechnical Microsystems

19 Packaging Technology for Microelectronics and Microsystems

20 Quality and Reliablility of Electronic Assemblies

21 Integrated Power Systems

Offers for Research and Service 23 Facilities and Equipment

23 Range of Services

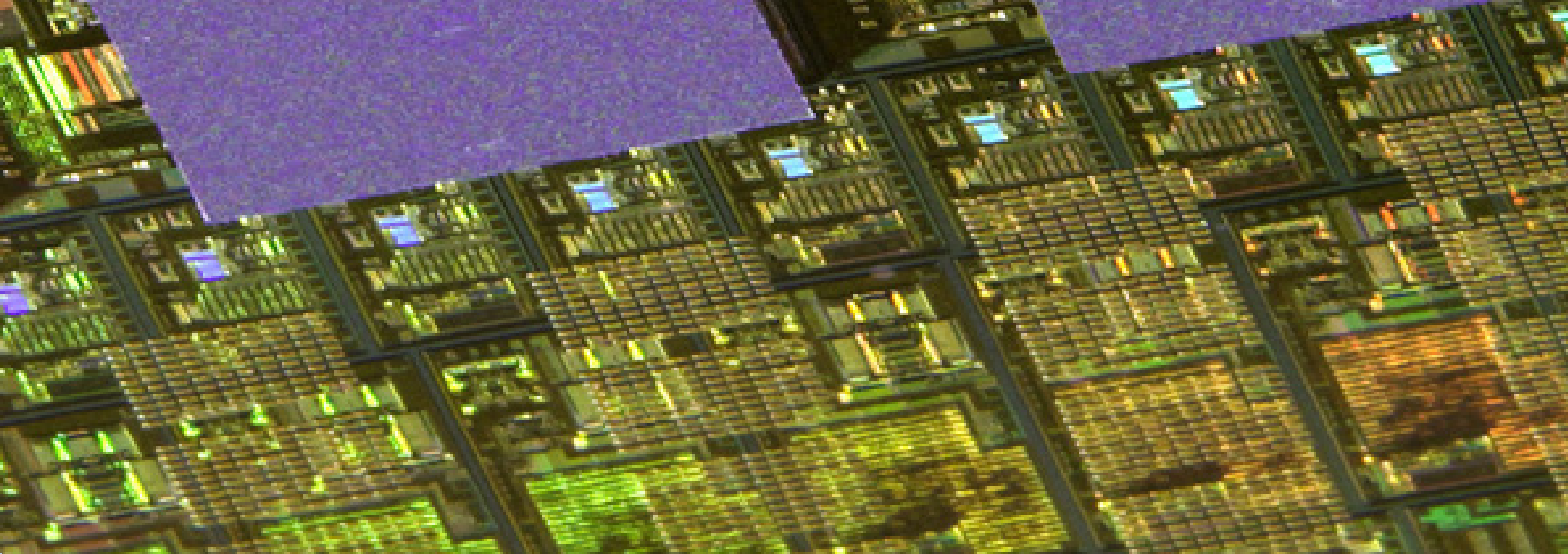
24 Customers

25 Innovation Catalogue

Representative Figures 28 Expenditure, Income, Staff Development

The Fraunhofer Gesellschaft 30 The Fraunhofer-Gesellschaft

31 Locations of the Research Establishment



REPRESENTATIVE RESULTS OF WORK

Microsystems Technology and IC-Design 34 Force/Torque Sensor for Robotic Industry

36 MEMS Based Multi Deflections Arrays for Parallel Shaped Electron Beam Lithography

40 MEMS Foundry Itzehoe GmbH

42 The Kiel Nano Laboratory

44 MEMSPACK – Zero- and First-level Packaging of RF-MEMS

48 Equipment Modernisation, Transfer to 8 Inch Production Technology

IC-Technology 50 PowerMOS Devices Custom-Designed for the Center of Competence for Power Electronics in Schleswig-Holstein

53 Super PowerMOS: Compensation Structures for High Voltage Applications

Biotechnical Microsystems 56 Point-of-Care-Diagnostic-Platform for HCV-Determination

Module Integration 60 Testwafers for Process Evaluation, Placement Accuracy and Reliability Tests

62 Electroless NiAu on Thinned Wafers Enables Cost Efficient Prototyping

64 Assessment of Thermal and Process Properties of Lead-Free Solder Pastes for High Reliable Electronic Devices

Integrated Power Systems 68 Lithium Storage in Silicon – Joint activity of ISIT and Technische Fakultät der Christian-Albrechts-Universität Kiel

Names, Data, Events 74 Lecturing Assignments at Universities

74 Memberships in Coordinationboards and Committies

75 Cooperation with Institutes and Universities

76 Distinctions

76 Trade Fairs and Exhibitions

77 Miscellaneous Events

Scientific Publications 78 Journal Papers and Contributions to Conferences

79 Diploma Theses

79 Patents

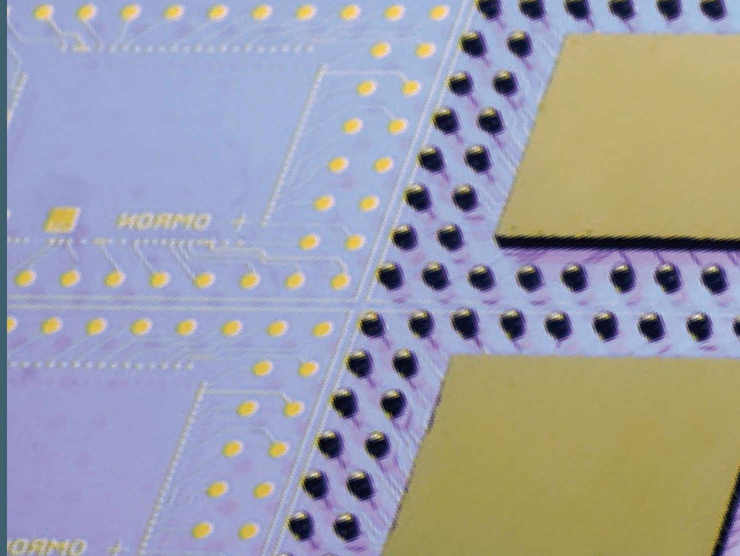
80 Talks and Poster Presentations

82 Overview of Projects

Imprint 84

Contact 85

PREFACE



Dear business partners, friends of the ISIT and colleagues,

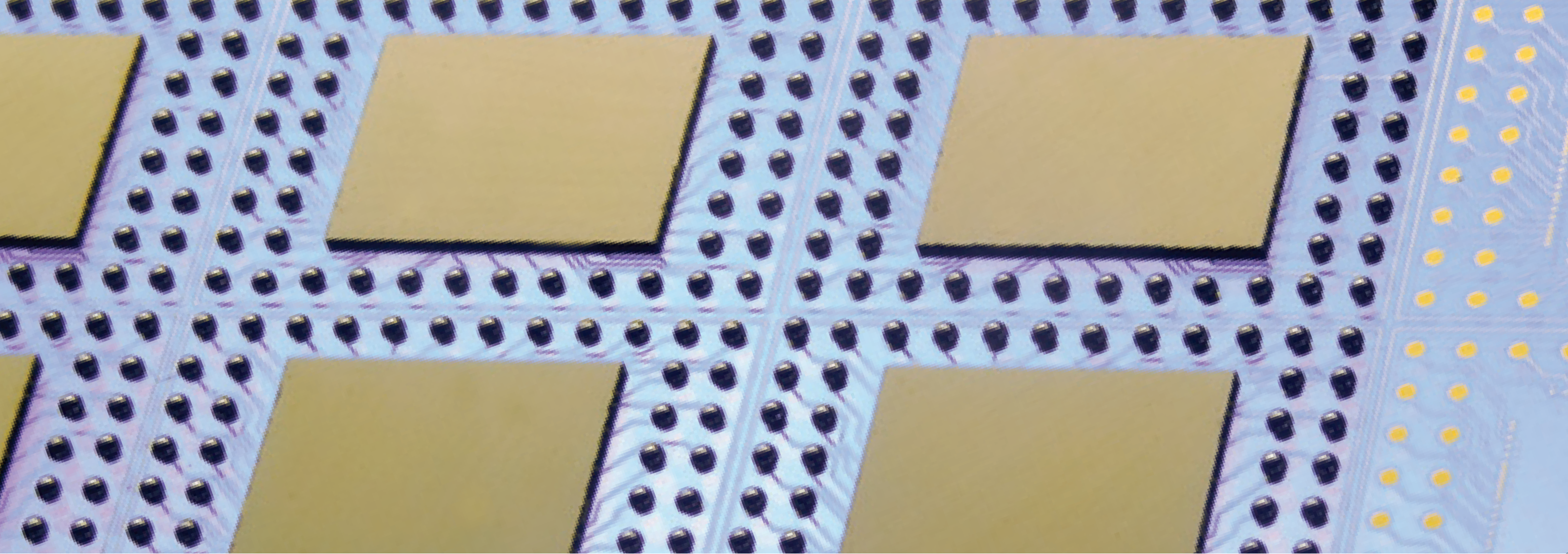
in the past year, Fraunhofer ISIT has delivered many much needed solutions to technological problems that also affect society as a whole. A variety of issues relating to energy and energy efficiency were dealt with in numerous projects, for the most part together with industrial partners.
This enabled us to advance our policy of consolidation by concentrating human and technical resources in the areas of most importance. Overall, 2009 was a year in which we had to face up to the challenges of a distinctly weakened global economy and difficult funding conditions. Nevertheless, thanks to solid working relationships with our customers in industry and public administration, the institute was able to generate sufficient revenues to meet its business and research targets for the year. I would therefore like to express my gratitude to all concerned for the trust they have placed in the institute and for their positive collaborative input.
In particular, my thanks go to our industrial customers, our partner institutes within the Fraunhofer-Gesellschaft and in the academic research community, the federal and Länder ministries, and other research funding agencies including individual project sponsors and the EU.
We also wish to express our gratitude to the Fraunhofer Executive Board along with the central administrative departments and the coordination officer in charge of our institute. And not least I wish to thank the institute staff for their dedicated efforts, without whom we would not have been able to achieve our targeted results.

In 2009, Fraunhofer ISIT focused its efforts on consolidating its resources and the store of expertise acquired over the years, giving priority to interdisciplinary collaboration in the fields of power electronics, power generation and distribution, and energy efficiency. By doing so, we have defined a common strategy for future activities in the fields of

Liebe Geschäftpartner, Freunde des ISIT und Kollegen,

*bei der Lösung drängender, auch gesamtgesellschaftlich bedeutsamer Probleme, konnte das Fraunhofer ISIT im zurückliegenden Jahr wichtige Beiträge liefern.
Bei vielen Fragestellungen um die Themenfelder Energie und Energieeffizienz wurden erfolgreich Projekte überwiegend mit Partnern aus der Industrie platziert und bearbeitet. Hierdurch konnte die weitere Fokussierung der Ressourcen und Kompetenzen in diesen Bereichen weiter vorangetrieben und konsolidiert werden. Das Jahr 2009 war global durch ausgesprochen schwierige wirtschaftliche Rahmen- und Randbedingungen geprägt. Die gute Zusammenarbeit mit unseren industriellen Kunden und öffentlichen Auftraggebern führte dennoch im Ergebnis zu einer erfreulichen Ertragslage für das Institut, so dass die für das Jahr formulierten Ziele konsequent verfolgt werden konnten. Für das entgegengebrachte Vertrauen und die konstruktive Zusammenarbeit möchte ich an dieser Stelle allen Beteiligten danken. Dies gilt in ganz besonderem Maße für unsere industriellen Auftraggeber, unsere Partner innerhalb der Fraunhofer-Gesellschaft und im universitären Umfeld, den Ministerien und Förderinstitutionen in Land und Bund, den Projektträgern und der EU und dem Fraunhofer-Vorstand mit der Zentralverwaltung und dem Institutsbetreuer.
Ohne das engagierte Wirken all unserer Mitarbeiter wäre allerdings das erzielte Ergebnis nicht erreichbar gewesen, was ich auf diesem Wege anerkennen möchte.*

Das Fraunhofer ISIT hat sich im zurückliegenden Jahr darum bemüht die Ressourcen und das über viele Jahre erworbene Know-how weiter zu bündeln und durch abteilungsübergreifende Zusammenarbeit auf die Themenfelder Leistungselektronik, Energie und Energieeffizienz zu konzentrieren. Auf diesem Wege ist eine

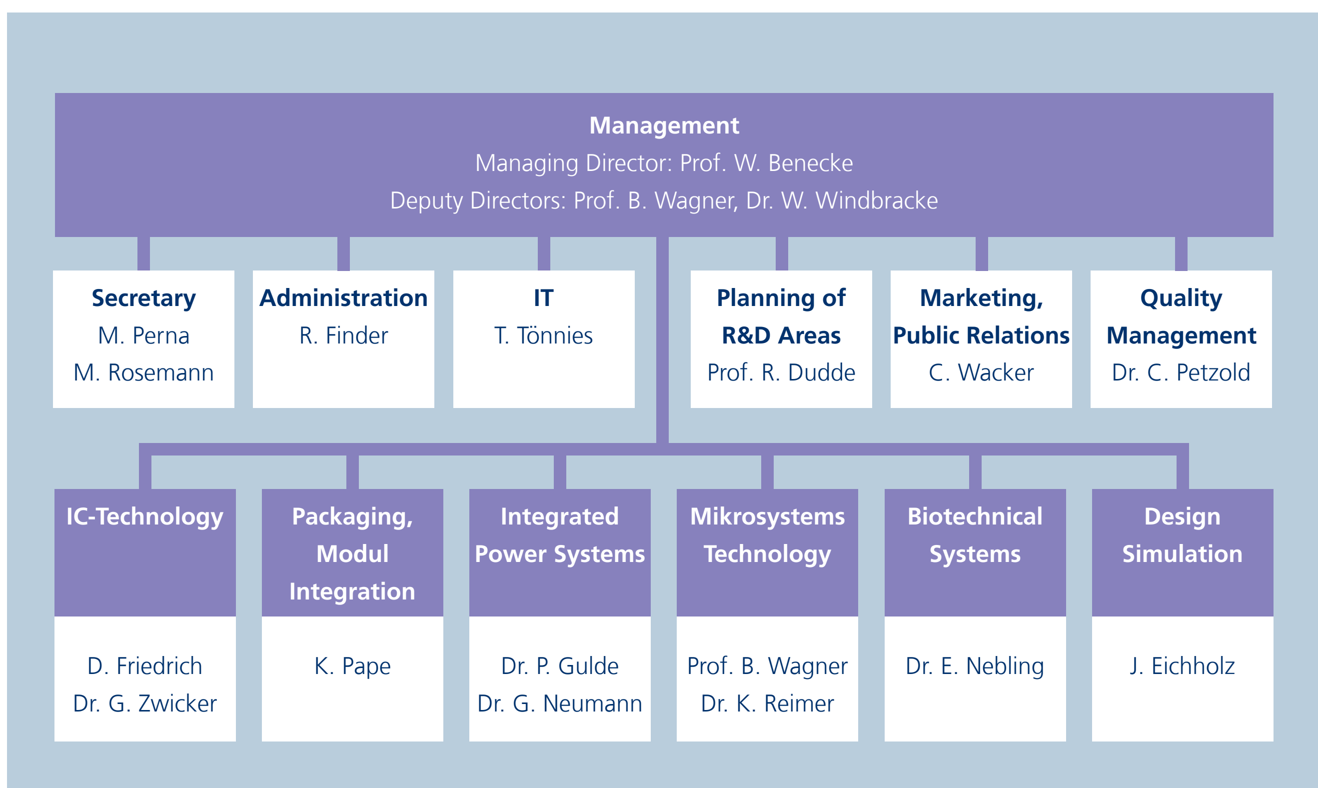


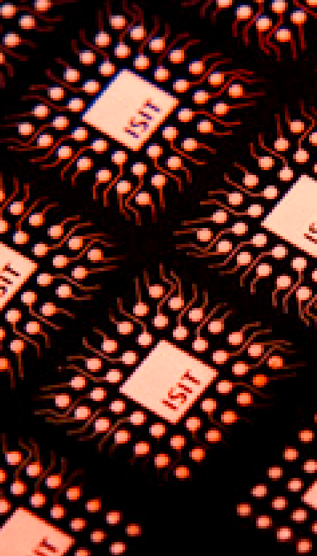
Flip chip on glass technology for image sensors

IC technology, integrated power systems, IC design, packaging technology, quality/reliability and micro/ nanosystems technology (MEMS). We aim to advance further in these areas by intensifying our development of application specific know-how in the corresponding applications. We have established a project to this effect in close consultation with the Executive Board of the Fraunhofer-Gesellschaft. Its emphasis lies on the outstanding technological capabilities of ISIT, which promise to furnish the

gemeinsame Klammer für die Abteilungen IC-Technologie, Integrierte Energiesysteme, IC Design, Aufbau- und Verbindungstechnik, Qualität und Zuverlässigkeit bis hin zur Mikro- und Nanosystemtechnik (MEMS) entwickelt worden. Dieser Weg soll gefestigt und gezielt durch die vertiefte Erarbeitung von Anwendungs-Know-How gestärkt werden. In enger Abstimmung mit dem Vorstand der Fraunhofer-Gesellschaft konnte hier ein entsprechendes Projekt ins Leben gerufen werden. Dabei

ISIT-Organigramm





Testwafer for Through-Silicon Via

Dr. Peter Merz, MFI, demonstrates microsensors to Minister President Peter Harry Carstensen

Thomas Rachel, Parliamentary State Secretary, Dr. Rolf Koschorrek, MdB, and Prof. Wolfgang Benecke presenting the second ISIT cleanroom building conception

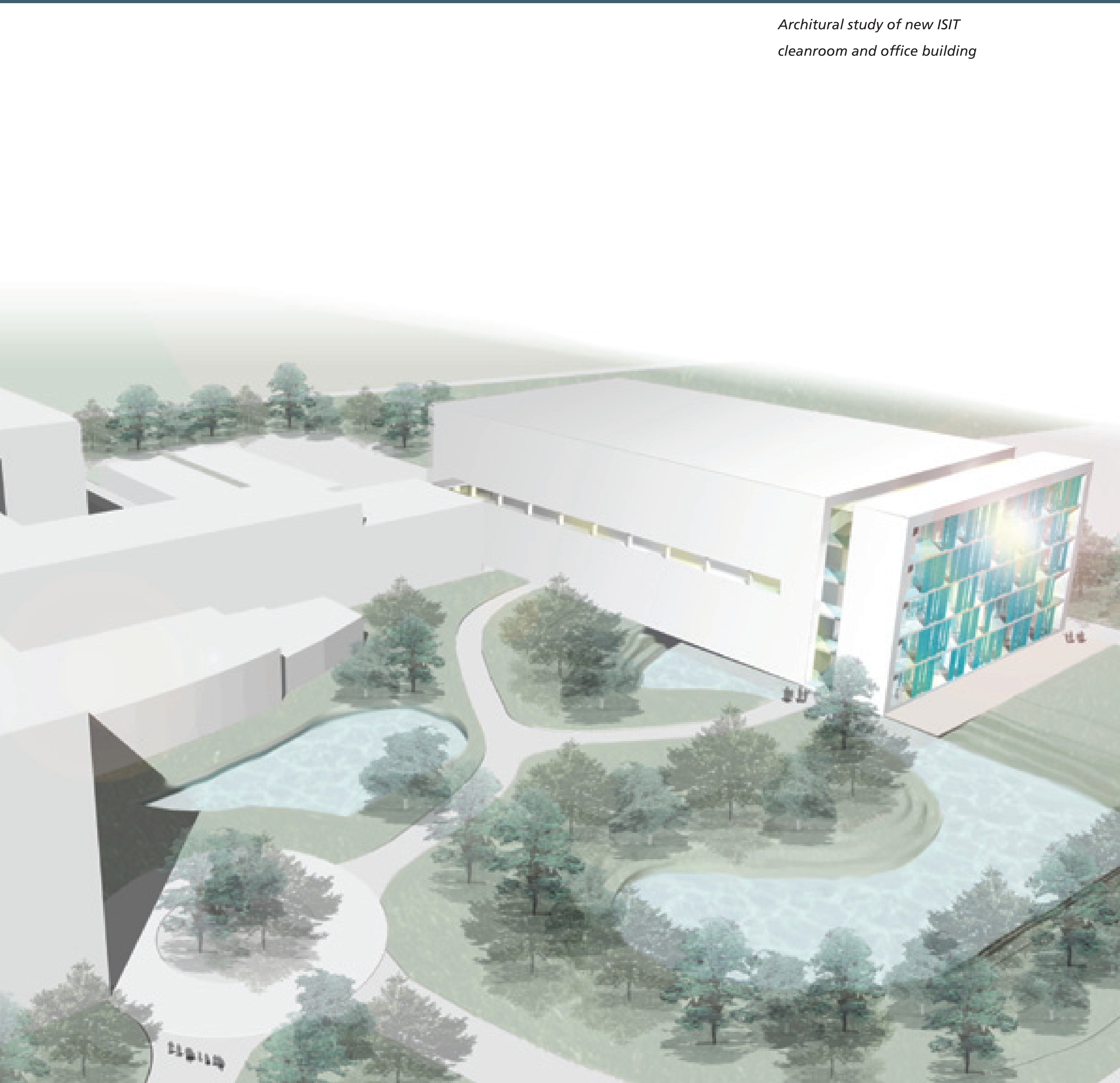
institute and its partners in the Fraunhofer networks with a strong competitive advantage – and in some cases even unique selling points – in the international market. Particularly strong growth was recorded in the field of battery systems, where there is a huge unmet need for innovative storage systems for electrical energy. Research in this context focused on applications relating to electromobility (Fraunhofer System Research for Electromobility FSEM) and on promoting the industrial use of renewable energy sources. The acquisition of a pilot plant for the manufacture of lithium-polymer batteries has opened up excellent opportunities for ISIT in this respect.

As part of longer-term plans to secure the ISIT's competitiveness, work continued and was to a large extent completed on the conversion and expansion of technological facilities to process 200 mm (8 inch) wafers. Investment capital of € 10.4 million (75 % Land Schleswig-Holstein, 25 % Fraunhofer-Gesellschaft) was allocated to the creation of a closed process chain for micro- and nanoscale engineering applications based on 200 mm diameter wafers. With this technology platform, ISIT now has one of the most advanced R&D facilities of this kind, even by international standards, and is thus ideally equipped to engage in further successful collaboration with companies and other research institutions in the field of microsystems and nanosystems engineering.
A related positive aspect is that the institute has received the necessary approval to go ahead with additional expansion projects. The construction of a new building to accommodate cleanroom, laboratories and office facilities will help to eliminate the present capacity shortages and open the way to new opportunities for industrial cooperation. This construction project is meanwhile at the detailed planning stage, and every effort is being made to meet the completion target of 2012.

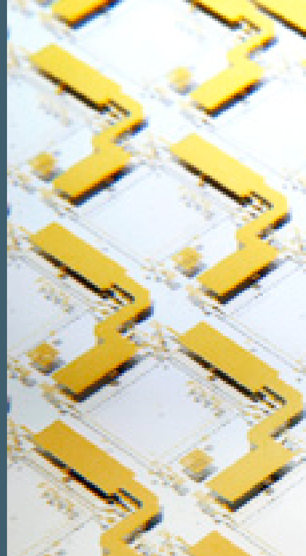
*werden die heraus-
ragenden Möglichkeiten des ISIT im Bereich der Technologie im Vordergrund stehen, da sie dem ISIT und auch seinen Partnern in den Fraunhofer Netzwerken besondere Vorteile im internationalen Wettbewerb verschaffen und z.T. Alleinstellungsmerkmale haben. Ein besonders starkes Wachstum war im Bereich der Batterieentwicklungen zu verzeichnen, da hier ein dramatischer Aufholbedarf bei der Entwicklung innovativer Speicher für elektrische Energie besteht. Die Arbeiten konzentrieren sich auf Anwendungen im Bereich der Elektromobilität (Fraunhofer Systemforschung Elektromobilität FSEM) und auf die Stärkung der Industrien im Bereich der regenerativen Energien. Die Beschaffung einer Pilotfertigungsanlage für Li-Polymer-Speicherzellen ermöglicht dem ISIT hier zukünftig herausragende Möglichkeiten.*

Für die langfristige Sicherstellung der Wettbewerbsfähigkeit des ISIT wurde im zurückliegenden Jahr die Umstellung und Erweiterung der Technologie auf die Bearbeitung von 200 mm-Wafer (8") betrieben und weitgehend abgeschlossen. Investitionen in Höhe von 10,4 Mio. € (75 % Land Schleswig-Holstein, 25 % Fraunhofer Gesellschaft) wurden eingesetzt, um eine geschlossene Prozesskette im Bereich der Mikro- und Nanosystemtechnik auf der Basis von 200 mm-Wafern zu schaffen. Das ISIT verfügt mit dieser Technologieplattform über eine, auch international betrachtet, der modernsten F&E Einrichtungen und ist somit bestens für die weitere erfolgreiche Zusammenarbeit mit Unternehmen und Institutionen auf dem Gebiet der Mikro- und Nanosystemtechnik aufgestellt. Erfreulich ist in diesem Zusammenhang die Bewilligung der weiteren Ausbauvorhaben. Durch den Bau eines weiteren Gebäudes mit Reinraum-, Labor- und Büroflächen

Architural study of new ISIT cleanroom and office building



Cartridge with electrical biochip



Glass substrate test wafer for ultrasonic flip chip assembly

The total cost of the project, amounting to approximately € 36 million, is being financed mainly by the Land of Schleswig-Holstein (approx. € 27 million, including EU funding) and partly by the Fraunhofer-Gesellschaft (approx. € 9 million). This project will further strengthen the technology platform for micro-systems and nanosystems engineering, ensuring its long-term future.

There is positive news to report in connection with the ISIT's cooperation with regional universities, which offers great promise for the future. The appointment of Prof. Wagner to the chair of Materials and Processes for Nanoscale Engineering at the University of Kiel (Christian-Albrechts-Universität zu Kiel, CAU) represents a major step forward in our efforts to establish a solid long-term basis for research in emerging areas of technology. ISIT is likewise directly involved in the DFG's newly created Collaborative Research Centre on "Magnetoelectric composites, the biomagnetic interfaces of the future" (CRC 855). A permanent working group is currently being set up at the nanotechnology laboratory attached to the University of Kiel's faculty of engineering. ISIT has also continued to nurture its collaborative ties with the universities of applied sciences in Schleswig-Holstein, with equally gratifying results.

ISIT has entered into a completely new dimension in its collaboration with customers through the creation of MEMS Foundry Itzehoe GmbH MFI. The company produces micro-electromechanical systems (MEMS) at the Itzehoe site to customer specifications, thus following on seamlessly from the research and development services provided by ISIT. Given the complexity of engineering solutions and technologies required to develop and manufacture microsystems and nanosystems, the co-location

werden die bestehenden Engpässe beseitigt und neue Möglichkeiten für Industriekooperationen geschaffen. Die Detailplanungen für die Ausbaumaßnahme wurden begonnen und mit dem Ziel der Fertigstellung im Jahre 2012 vorangetrieben. Von den Kosten in Höhe von etwa 36 Mio. € trägt das Land Schleswig-Holstein etwa 27 Mio. €, EU-Mittel eingeschlossen, und die Fraunhofer Gesellschaft etwa 9 Mio. €. Mit diesem Vorhaben wird die Technologieplattform für Mikro- und Nanosystem-technik weiter gestärkt und langfristig gefestigt.

Vielversprechend und positiv hat sich die Zusammen-arbeit des ISIT mit den regionalen Hochschulen entwickelt. Durch die Berufung von Herrn Prof. Wagner auf den Lehrstuhl für Materialien und Prozesse der Nanosystemtechnik der Christian-Albrechts-Universität zu Kiel (CAU) konnte ein wichtiger Schritt zur langfristigen Sicherung von Zukunftsthemen vollzogen werden. So ist das ISIT auch in den neu eingerichteten Sonder-forschungsbereich SFB 855 „Magnetoelektrische Verbundwerkstoffe – Biomagnetische Schnittstellen der Zukunft" direkt eingebunden. Mit dem Aufbau einer permanenten Arbeitsgruppe am Kieler Nanolabor der Technischen Fakultät der CAU wurde begonnen. In gleicher Weise positiv konnten auch die bestehenden Kooperationen mit den Fachhochschulen im Land fortgeführt werden.

Eine völlig neue Qualität in der Zusammenarbeit zwischen dem ISIT und seinen Kunden wurde mit der Gründung der MEMS Foundry Itzehoe GmbH (MFI) geschaffen. Das Unternehmen führt im Auftrag von Kunden die Produktion von MEMS am Standort Itzehoe durch und schließt damit lückenlos an die von ISIT erbrachten F&E Leistungen an. Durch die inzwischen hohe technische und technologische Komplexität von

ISIT's Managing Director
Prof. W. Benecke

of development and production facilities is a strongly appealing concept – all the more so in the light of the increasing pressure to cut lead times and costs. MFI's creation is thus a logical step that provides ISIT with a new means of attracting customers and winning bids for projects, combining all stages of advanced system development from strategic, pre-competitive research to production in a single location.

To conclude, I would like to thank all customers and research sponsors once again for the trust they have placed in the ISIT. The institute offers an outstanding infrastructure in which to develop new and innovative systems.

We invite you to profit from the specialized knowledge we have built up over the decades and make use of the excellent technical facilities we have to offer. You are welcome to contact us at any time you need advice on specific problems or tasks.

We look forward to working with you again.

Mikro- und Nanosystemen ist die Durchführung von Entwicklung und Produktion am selben Standort ein sehr attraktives Konzept. Der wachsende Zeit- und Kostendruck verstärkt diesen Umstand weiterhin. Die Gründung der MFI ist daher konsequent und schafft für das ISIT neue Möglichkeiten der Kundengewinnung und der Projektakquisition, da alle Aspekte der fortgeschrittenen Systementwicklung von der strategischen Vorlaufforschung bis hin zur Produktion am Standort verfügbar sind.

Abschließend möchte ich noch einmal allen Kunden und Förderern des ISIT für das entgegengebrachte Vertrauen danken. Das Institut ist für die Entwicklung neuer und innovativer Systeme bestens aufgestellt.

Nutzen Sie das über Jahrzehnte geschaffene Wissen und die hervorragenden technischen Möglichkeiten. Wir sind jederzeit für Sie ansprechbar, um Problem- und Aufgabenstellungen zu beraten.

Wir freuen uns auf die Zusammenarbeit mit Ihnen.

W. Benecke

Fraunhofer ISIT in Itzehoe: cleanroom and office building

FRAUNHOFER-INSTITUT FÜR SILIZIUMTECHNOLOGIE (ISIT)

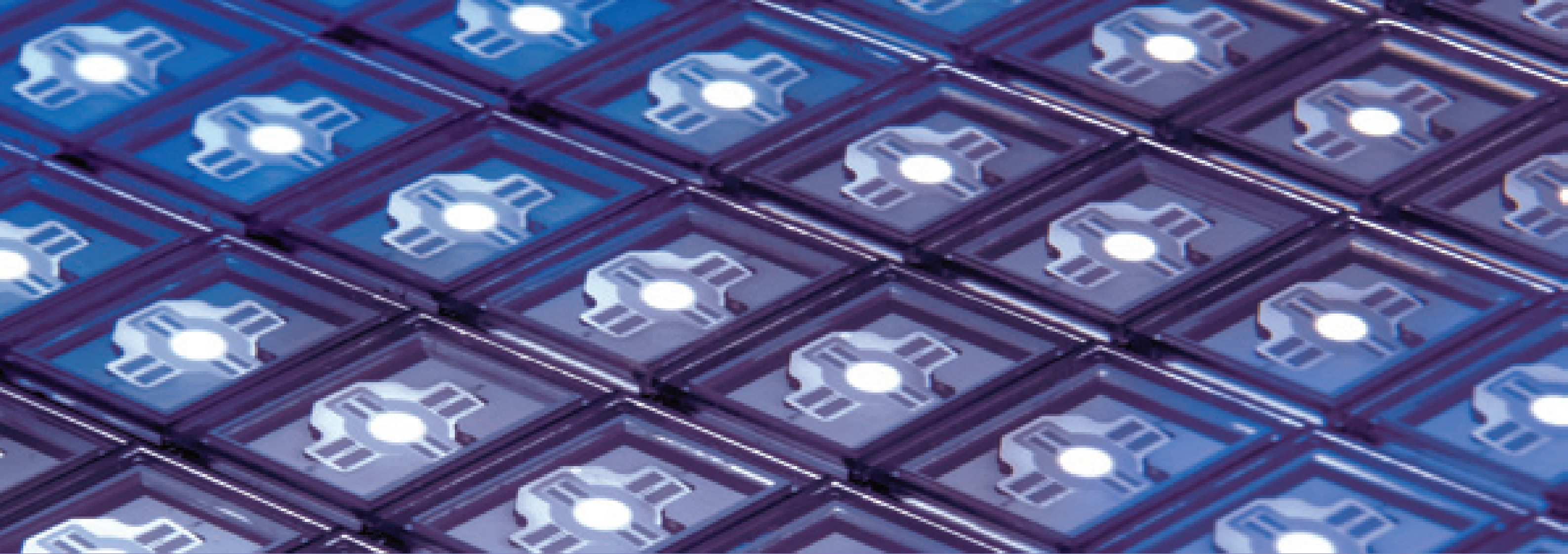
Research and Production at one Location

The Fraunhofer-Institut für Siliziumtechnologie (ISIT) develops and produces microelectronic components with focus on power electronics and microsystems. The advanced process line based on a 200 mm silicon wafer technology and the expertise built up over decades ensure a world-leading position for ISIT and its customers. Microcomponents for a wide range of applications are developed by the institute. The main areas of application are automotive and transport engineering, consumer goods industry, medical technology, communication systems and automation. ISIT carries out the design and system simulation of microcomponents for its customers and provides prototypes and pilot production, provision of samples and preparation of series production.

The institute also offers design expertise on application-specific integrated circuits (ASICs) for the operation of sensors and actuators and deals with all the important tasks involved in system integration, assembly and interconnection technology (packaging) and the reliability and quality of components, modules and systems. Activities are completed by intensive development work on electrical energy storage devices based on Lithium polymer batteries.

MAIN FIELDS OF ACTIVITY

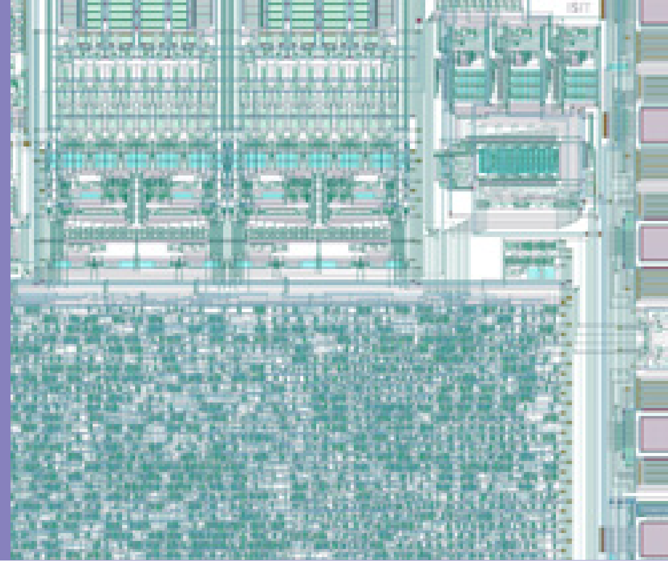
ISIT frontend cleanroom: vertical furnaces



MICROSYSTEMS TECHNOLOGY (MEMS) AND IC DESIGN

Demonstrator for an inertial measurement unit (IMU)

Waferlevel packaged two axis micromirrors developed for laser projection



IC Layout to drive a DC brushless motor

Research in microsystems technology is a core activity of Fraunhofer ISIT in different departments. For more than 25 years ISIT scientists are working on the development of micro electro mechanical systems (MEMS). This covers the complete spectrum starting from simulation and design, technology and component development up to development of endtest strategies and reliability tests. One of the core competences of the ISIT service offer is the development of integration technologies, like cost effective assembly of several chips in a common package, MEMS packaging on waferlevel (WLP) with defined cavity pressure or a system-on-chip approach. MEMS devices can be combined with a suitable ASIC to miniaturized systems with high functionality.

The ISIT cooperation model allows further to offer also a fabrication of prototypes and starting a pilot production. If high volume MEMS production is requested the on-site operating industrial partner MEMS Foundry Itzehoe (MFI) is able to meet this demand.

ISIT is focussed on MEMS applications in three core areas: physical sensors and actuators, devices and technologies for high frequency application (RF-MEMS) as well as passive and active optical microsystems.

In the field of sensor systems strong activities are put on inertial sensors (accelerometer, gyrometer, IMUs) and on flow sensors with integrated electronics (ASICs) respectively. Special technological process modules for sensor development are available, e.g. thick poly silicon as a functional layer or hermetic encapsulation on waferlevel.

High frequency microsystems at ISIT are primarily for application in wireless reconfigurable communication networks, in particular developments for RF-MEMS switches, ohmic switches and waferlevel packaging are running.

In the field of optical MEMS devices ISIT is active in the development of micromirrors for laser projection displays, optical scanning systems and light modulators. Passive optical microsystems are also in the portfolio of ISIT, as there are glass lens arrays or aperture systems for laser beam intensity forming.

At ISIT a large number of single process technologies are available. These have been combined to specific qualified MEMS process modules. They work like a tool kit to realize several applications. Special attention is paid to the PSM-X2 process module, which is based on thick polysilicon layer for the fabrication of accelerometers or gyrometers with automotive qualification AEC Q100.

One of the prerequisites for the development of microsystems and microelectronic components is a highly capable integrated circuit design group. The staff at ISIT are specialists in the design of analog/digital circuits, which enable the electronic analysis of signals from silicon sensors. The designers also model micromechanical and micro optic elements and test their functionality in advance using FEM and behavioral modeling simulation tools.

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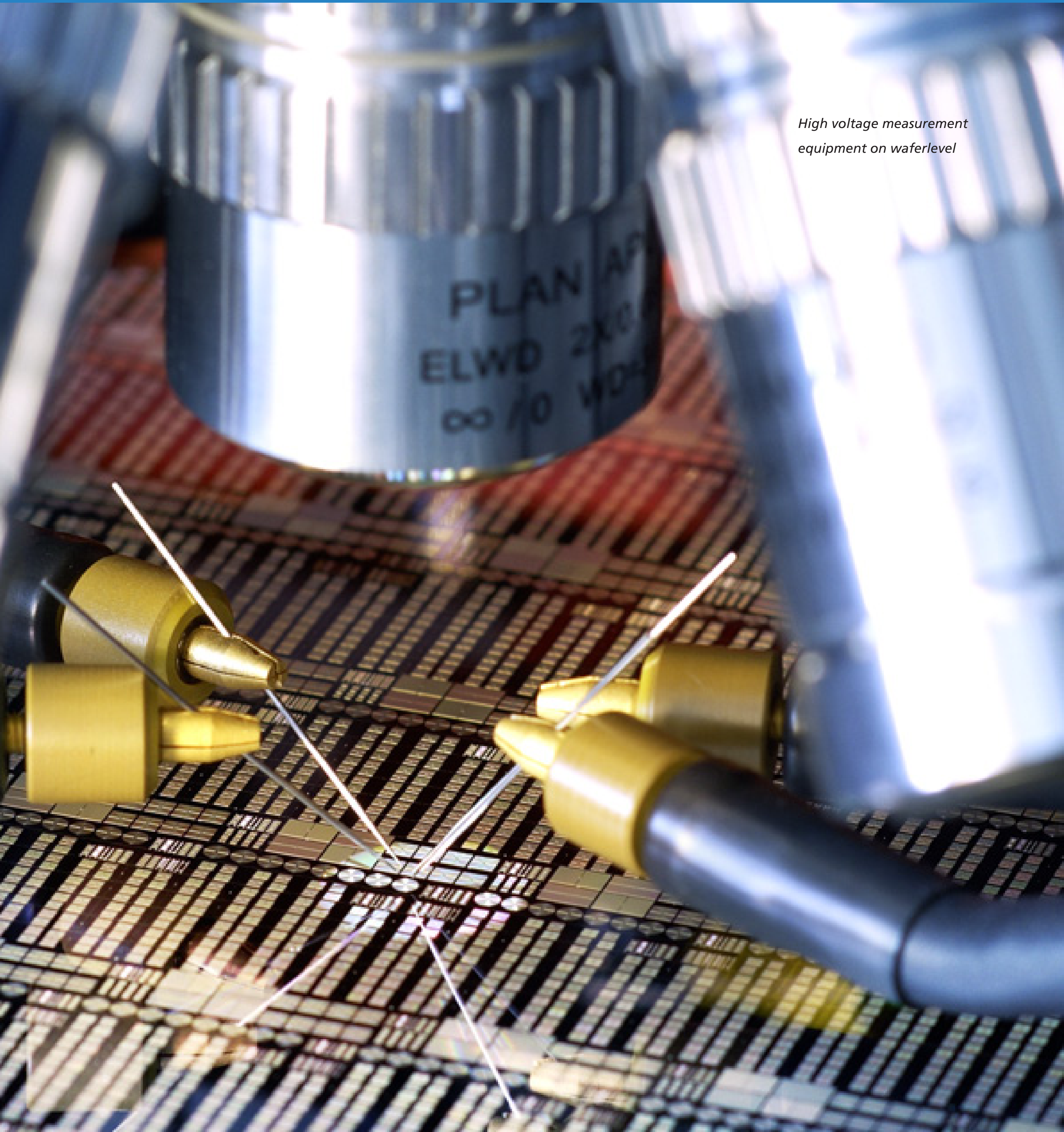
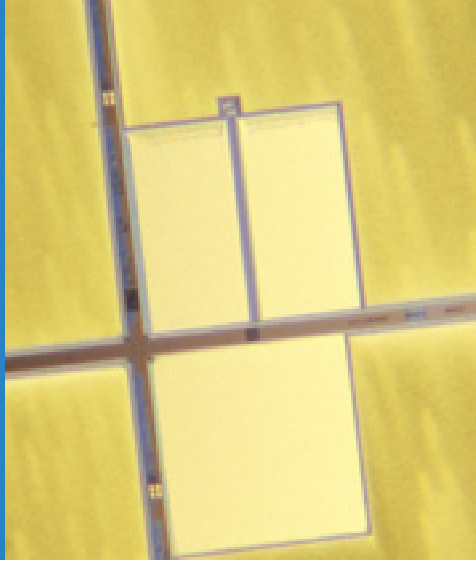
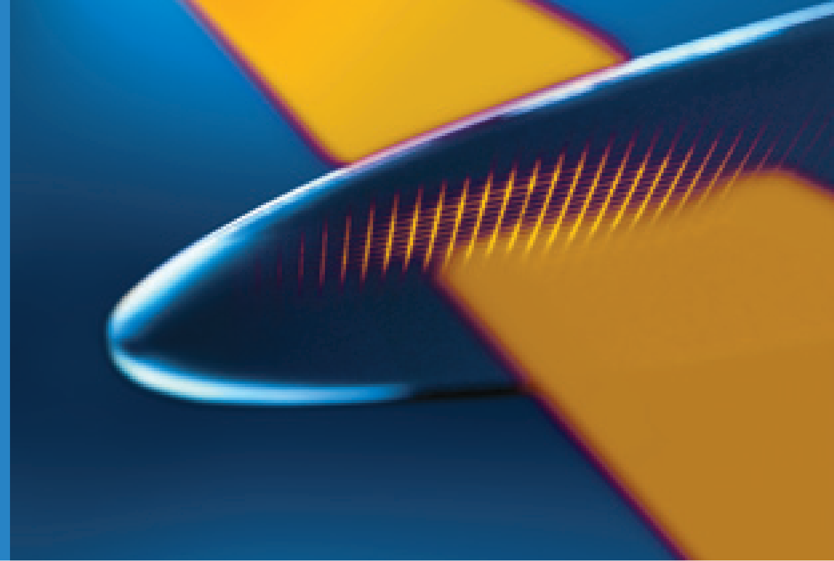
MAIN FIELDS OF ACTIVITY



High voltage measurement equipment on waferlevel



PowerMOS device with temperature sensor



Ultrathin PowerMOS wafer

IC TECHNOLOGY AND POWER ELECTRONICS

The power electronics and IC technology group develops and manufactures active integrated circuits as well as discrete passive components.

Among the active components the emphasis lies on power devices such as smart power chips, IGBTs, PowerMOS circuits and diodes. In this context application specific power devices and new device architectures are special R&D areas. The development of new processes for advanced power device assembly on waferlevel is a further important research topic. It comprises e. g. adapted chip metallization and novel techniques for backside processing of ultra thin Silicon substrates. Additional support is provided by a number of tools for simulation, design and testing. ISIT also benefits from years of experience in the design and manufacturing of CMOS circuits.

Passive components developed and fabricated at ISIT are primarily chip capacitors, precision resistors and inductors. Development of materials and the integration of new materials and alloys into existing manufacturing processes play an important role in the development process. ISIT develops individual processes, process modules and complete process flows for diverse applications. The institute also offers processing of customer-specific silicon components in small to medium-sized quantities on the basis of a qualified semiconductor process technology.

In the field of power electronics ISIT coordinates a competence center which was founded in close cooperation with universities and companies of the federal country Schleswig-Holstein. A special R&D group with focus on power electronic systems works on application specific topics covering the interface to system end users. To support the development of new semiconductor production techniques, production equipment of particular interest is selected for testing and optimization by the ISIT staff. This practice provides the institute with specialized expertise related to e. g. etching, deposition, lithography, and planarization methods. Planarization using chemical-mechanical polishing (CMP) in particular is a key technology for manufacturing advanced integrated circuits and microsystems. The intensive work done by ISIT in this area is supported by a corresponding infrastructure. A special emphasis lies in the application of CMP for the manufacturing of MEMS devices and microsystems. The institute's CMP application lab is equipped with CMP polishing machines and post-CMP cleaning equipment as well as the corresponding measurement tools for wafer diameters between 100 and 300 mm. The CMP group at ISIT works in close relationship to Peter Wolters AG since many years, as well as with other semiconductor equipment manufacturers, producers of polishing slurries and pads, CMP users and chip and wafer manufacturers.

The group's work encompasses the following areas:

- Testing of CMP systems and CMP cleaning equipment
- Development of CMP processes for
  - Dielectrics (SiO_2, TEOS, BPSG, low-k, etc.)
  - Metals (W, Cu, Ni, etc.)
  - Silicon (wafers, poly-Si)
- Testing of slurries and pads for CMP
- Post-CMP cleaning
- CMP-related metrology
- Implementation of customer-specific polishing processes for ICs and micro systems

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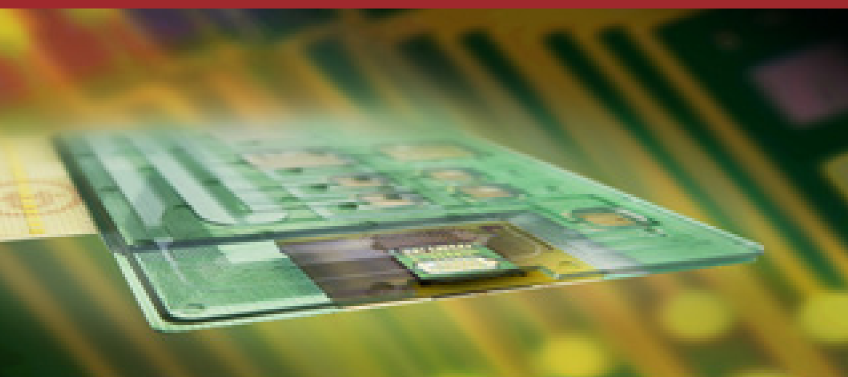
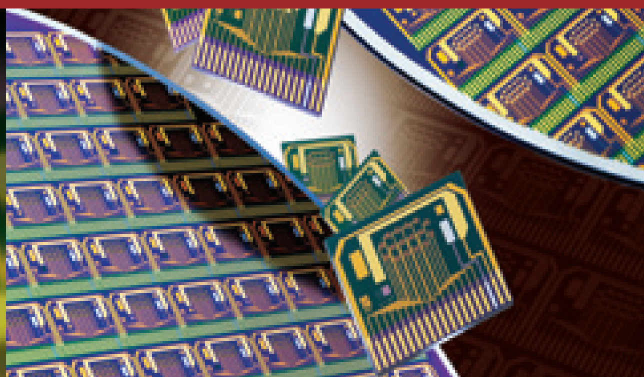


Fraunhofer ivD-cartridge equipped with electrical biochip, fluidic parts and reservoirs



Silicon based electrical biochips with microarray

BIOTECHNICAL MICROSYSTEMS

ISIT is one of the worldwide leaders at the field of electrical biochips. These chips allow the realization of very efficient biosensors and are the basis for fast and cost effective analytical systems.

The electrical biochip technology offers intrinsic advantages over optical biochips because of particle tolerance and mechanical robustness by the direct transduction of biochemical reactions into electrical current. The use of gold electrode arrays combined with integrated reference and auxiliary electrodes along with sensitive, selective measurement techniques like "Redox-Cycling" enables powerful sensor systems. These arrays are useful for the detection of a variety of analytes within one probe simultaneously. User-friendly operability is realized by integrating the biochips into cartridges. In combination with micro-fluidic components and integrated electronics, these electrical micro-arrays represent the basis of rapid and cost-effective analysis systems. They can be used to identify and quantify DNA, RNA, and proteins.

Further biosensors enable continuous monitoring, e.g. of metabolites as glucose or lactate. The measurement of these substances is realized by enzymatic conversion and electrochemical detection.

ISIT works closely with the Itzehoe based company AJ eBiochip GmbH (www.aj-ebiochip.com), an ISIT spin-off, to facilitate the marketing of these new technologies.

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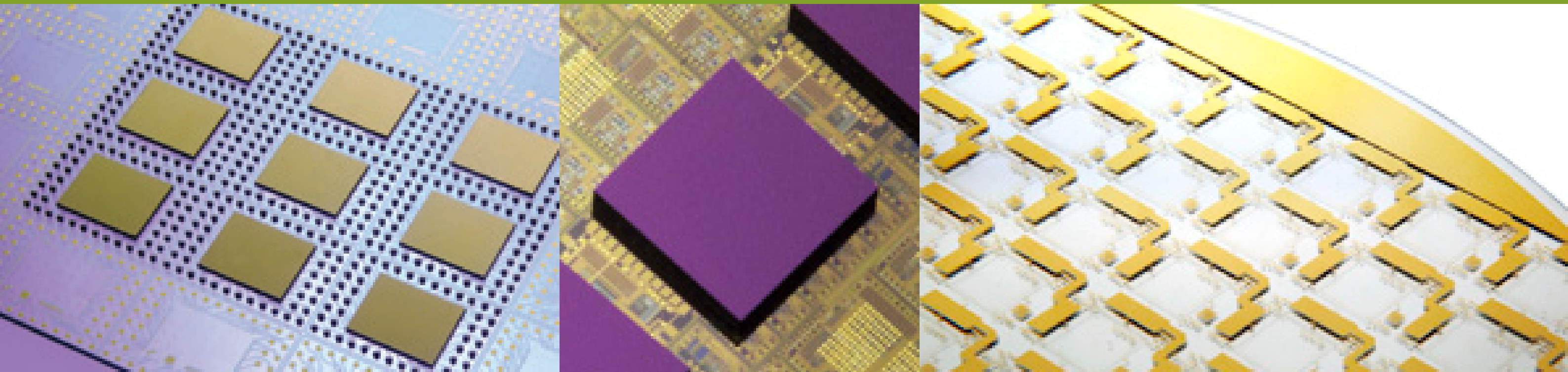

Glass wafers allow the integration of micro optic systems

Chip to wafer realization of vacuum packaged MEMS on ASIC

Testwafer for flip chip assembly on glass

PACKAGING TECHNOLOGY FOR MICROELECTRONICS AND MICROSYSTEMS

The "Advanced Packaging" group is specialized in detecting and promoting new trends and technologies in electronics packaging. The industrial challenges of tomorrow are addressed in direct collaboration with suppliers of materials, components, modules and equipment. As an example, the automatic pick-and-place assembly of thin dies on flexible substrates was already developed several years ago. For the encapsulation of MEMS components, the glass frit bonding was developed and later on replaced by the more efficient metallic bonding. ISIT equally participates in development activities on organic electronics and RFID technology.

The Fraunhofer ISIT disposes of all basic technologies for the automatic or manual handling of microchips and microsensors, as well as electrical interconnect methods like wire bonding and flip chip technologies.

Through the close relationship between MEMS technology and packaging in ISIT's premises, the institute has become a leading R&D service provider in the domain of waferlevel packaging. A cross-disciplinary technology portfolio is now available that allows to reduce cost and volume of a system. Even more, the packaging itself can become a functional part of the microsystem in many cases, e.g. by integrating optical elements or directly interconnecting MEMS and ASIC dies. Outstanding success was achieved in the vacuum encapsulation of micromechanical sensors by eutectic wafer bonding, which paved the way towards the industrialization of a gyro sensor product family for automotive applications.

ISIT continuously expands the assortment of test chips and -substrates that facilitate the ramp up and calibration of production lines for securing quality on a high level.

Packaging Technology for Microelectronics and Microsystems
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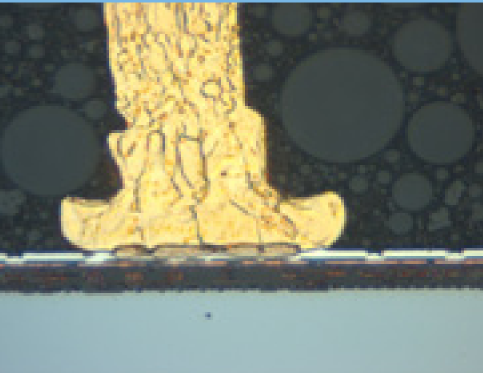
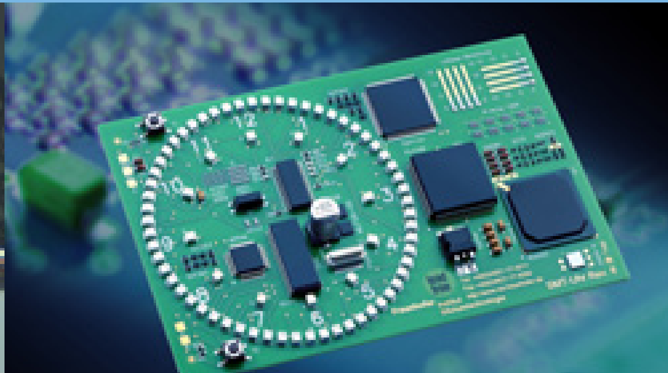
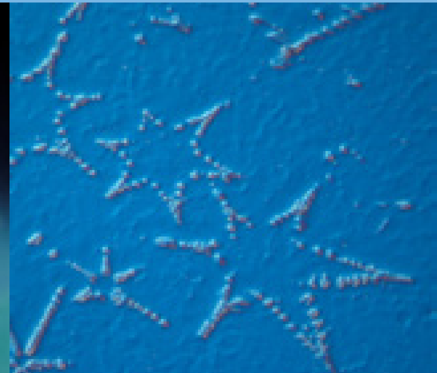


Gold wire bond Silicon chip



ISIT test board for soldering process evaluation



Solder microstructure

QUALITY AND RELIABILITY OF ELECTRONIC ASSEMBLIES

Quality evaluation – in particular for the soldering work done in pre-production, pilot and main series lots – represents a continuous challenge for ISIT, as for example whenever new technologies such as lead-free soldering are introduced, or when increased error rates are discovered, or if a customer desires to achieve competitive advantages through continual product improvement. To reveal potential weak points, ISIT employs both destructive and non-destructive analysis methods, such as X-ray transmission radiography and scanning acoustic microscopy. Working from a requirements matrix, ISIT scientists also evaluate long-term behavior of lead-free and lead-containing assemblies alike. They then formulate prognoses on the basis of model calculations, environmental and time-lapse load tests, and failure analysis.

In anticipation of a conversion to lead-free electronics manufacturing, Fraunhofer ISIT is undertaking design, material selection and process modification projects for industrial partners. To effect a further optimization of manufacturing processes, the institute applies process models and produces samples on industry-compatible equipment. The group also addresses issues related to thermal management and reliability for customer-specific power modules.

In addition to these technological activities, the group regularly holds training sessions, including multi-day classes, at the institute or at company site.

Quality and Reliability of Electronic Assemblies
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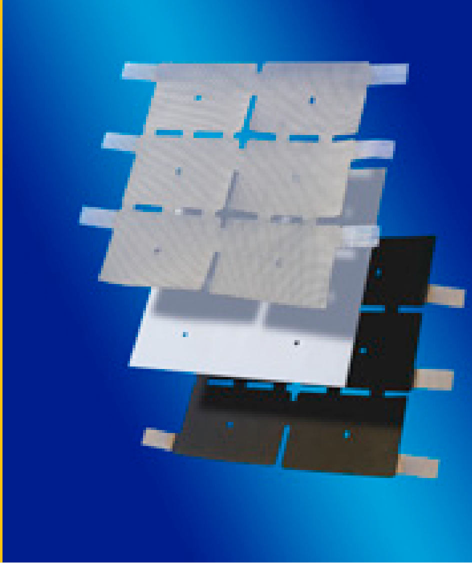

Punched electrode foils and separator for Lithium Ion batteries

Electrolyte filling of Lithium Ion batteries in an Argon atmosphere glovebox

INTEGRATED POWER SYSTEMS

These new fields include automobiles, medical devices, stationary electric storage units, aerospace, etc. Therefore, this type of rechargeable batteries has to meet a variety of new requirements. This covers not only electrical performance but also design and safety features. The Lithium polymer technology developed at ISIT is characterized by an extensive adaptability to specific application profiles like extended temperature range, high power rating, long shelf and/or cycle life, extended safety requirements, etc. Also included is the development of application-specific housings.

In the Lithium polymer technology all components of the cell from electrodes to housing are made from tapes. At ISIT the complete process chain starting with the slurry preparation over the tape casting process and the assembly and packaging of complete cells in customized designs is available including also the electrical and thermo-mechanical characterization. This allows access to all relevant parameters necessary for an optimization process. The electrode and the electrolyte composition up to the cell design can be modified.

In addition to the development of prototypes, limited-lot manufacturing of optimized cells on a pilot production line at ISIT with storage capacities of up to several ampere-hours is possible.

Specific consideration in process development is addressed to the transferability of development results in a subsequent industrial production.

ISIT offers a wide portfolio of services in the field of secondary Lithium batteries:

- Manufacturing and characterization of battery raw materials by half cell as well as full cell testing
- Selection of appropriate combinations of materials and design of cells to fulfil customer requirements
- Application driven housing development
- Test panel
- Prototyping and limited-lot manufacturing of cells

Additional services are:

- Preparation of studies
- Failure analysis
- Testing (electrical, mechanical, reliability etc.)
- Technical consultation

Integrated Power Systems

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OFFERS FOR RESEARCH AND SERVICE

ISIT cleanroom:
optical wafer inspection

FACILITIES AND EQUIPMENT

ISIT operates in collaboration with Vishay Siliconix Itzehoe GmbH a semiconductor production line for 200 mm (8”) Si wafers (cleanroom area 2.500 m²). The process line is used for the development of new components and processes as well as for the production of components (PowerMOS, MEMS). Further cleanrooms (650 m²) are available for specific processes, as needed for example in microsystem engineering, and for chemical-mechanical polishing (CMP). In addition to the basic processes of microsystem engineering, highly developed processes are maintained, e.g. for high-precision deep etching (DRIE), deposition of non-IC-compatible materials such as piezoelectrics, thick-layer lithography and electroplating, glass molding and grey-scale lithography.

The institute has particular expertise in wafer bonding and waferlevel packaging (WLP), achieving unique levels of quality for various MEMS components (gyroscopes, scanner mirrors, RF-MEMS, etc.). Further laboratory areas (1.500 m²) are equipped for characterization, qualification and assembly and interconnection technology. The scope of activities is widened by laboratories for the development of Lithium polymer batteries, in which a pilot production plant is operated for sample production and evaluation tasks. To expand the institute’s capacity, a further cleanroom and laboratory building is planned, which is scheduled for completion in mid-2012. The ISIT’s facilities are certified to ISO 9001-2008.

RANGE OF SERVICES

Fraunhofer ISIT has many years of experience in industrial collaboration. Primarily the concept of technology platforms is pursued, i.e. the definition of process procedures in which the customer-specific solutions take place through the design and packaging. This allows to offer services which, beyond the technical specifications, are attractive in terms of risk, development time, development expense and production cost. Series production can ultimately be carried out in close cooperation with the locally based MEMS Foundry Itzehoe GmbH (MFI).

CUSTOMERS

ISIT cooperates with companies of different sectors and sizes.
In the following some companies are presented as a reference:

Aardex, *Zug, Switzerland*

ABB, *Västerås, Sweden*

ABB, *Ladenburg*

Ablestik, *Cambridge, England*

Accretech Europe GmbH, *München*

adaptif PHOTONICS GmbH, *Hamburg*

AEMtec, *Berlin*

Airbus-Systeme, *Buxtehude*

AJ eBiochip Systems GmbH, *Itzehoe-Jena*

Alcatel Vacuum Technology, *Annecy, France*

Alma, *Lyon, France*

Amic, *Uppsala, Sweden*

Andus electronic GmbH, *Berlin*

Applied Materials, ICT, *München*

ARC Seibersdorf Research GmbH, *Seibersdorf, Austria*

ASE, *Seoul, Korea*

Atmel Germany GmbH, *Heilbronn*

Atos Origin, *Madrid, Spain*

Atotech Deutschland GmbH, *Berlin*

Audi Electronics Venture GmbH, *Ingolstadt*

BASF SE, *Ludwigshafen*

Basler Vision Technologies, *Ahrensburg*

BIONT, *Bratislava, Slovakia*

B. Braun, *Melsungen*

Bundeswehr WTD, *Eckernförde*

CDTA, *Algier, Algerien*

Condias GmbH, *Itzehoe*

Conti Temic, *Karben*

Conti Temic microelectronic GmbH, *Nürnberg*

DancoTech A/S, *Ballerup, Denmark*

Danfoss Drives, *Graasten, Denmark*

Danfoss Silicon Power GmbH, *Schleswig*

Datacon Technology AG, *Radfeld/Tirol, Austria*

Evonik Degussa GmbH, *Hanau*

Delong Instruments a.s., *Brno, Czech Republic*

Diehl Avionik Systeme GmbH, *Überlingen*

Digisound-Electronic GmbH, *Norderstedt*

Dräger Systemtechnik, *Lübeck*

EADS Deutschland GmbH, *Corporate Research Germany, München and Ulm*

EN Electronic Network, *Bad Hersfeld*

Engineering Center for Power Electronics GmbH, *Nürnberg*

EPCOS, *Nijmegen, Netherlands*

ESCD, *Brunsbüttel*

ESW-Extel Systems GmbH, *Wedel*

EVGroup, *Schärding, Austria*

Flextronics, *Althofen, Austria*

Freudenberg & Co. KG, *Weinheim*

Fujitsu Siemens Computers GmbH, *Augsburg*

GE Healthcare, *Finland*

GPS GmbH, *Stuttgart*

Güdel AG, *Langenthal, Switzerland*

Hannusch Industrieelektronik, *Laichingen*

Harman & Becker, *Karlsbad*

Hasenkamp Internationale Transporte GmbH, *Köln*

Heidenhain, *Traunreut*

Hella KG, *Lippstadt*

Honeywell GmbH, *Schönaich*

HPL S.A., *Lausanne, Switzerland*

ifm electronic GmbH, *Essen*

IMS Nanofabrication AG, *Wien, Austria*

Jenoptik Innovavent GmbH, *Göttingen*

Jungheinrich AG, *Norderstedt*

Kaco Gerätetechnik GmbH, *Kassel*

Kavlico GmbH, *Minden*

Kristronics GmbH, *Harrislee-Flensburg*

Kuhnke GmbH, *Malente*

Lam Research, *Fremont, USA*

Leclanché Lithium GmbH, *Willstätt*

Lenze Drive Systems GmbH, *Hameln*

Liebherr Elektronik, *Lindau*

Litef, *Freiburg*

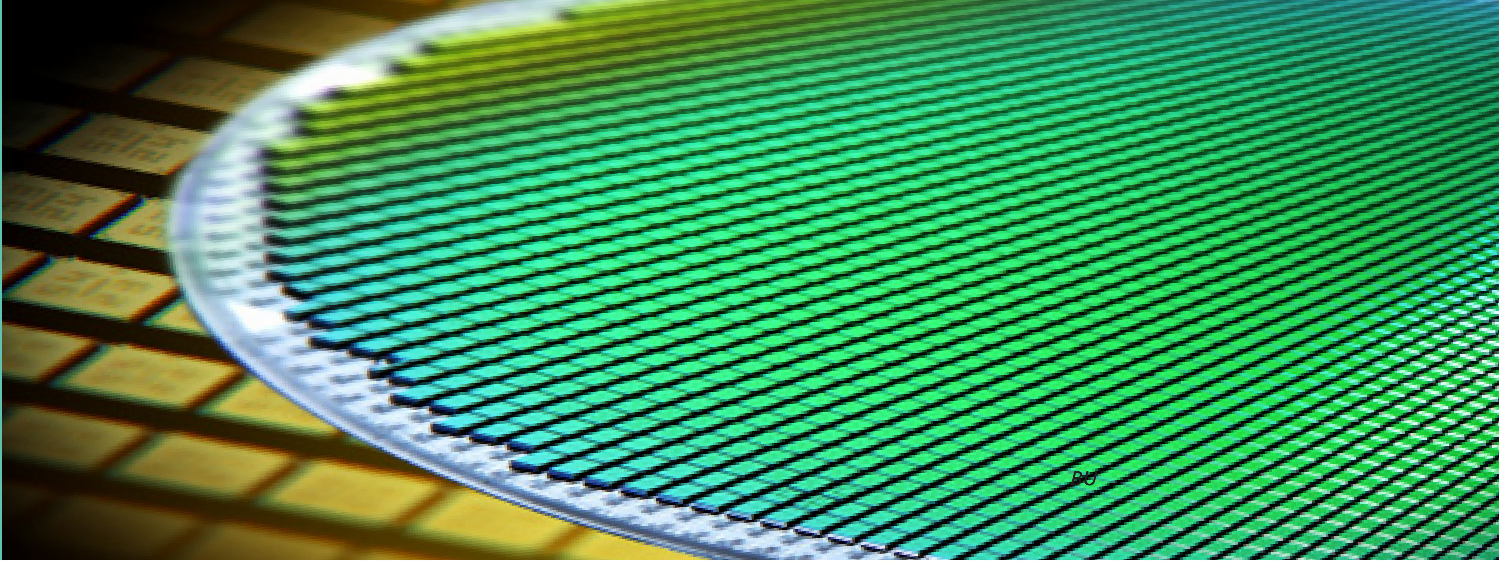
Lumio Ltd, *Jerusalem, Israel*

Mair Elektronik GmbH, *Neufahrn*

Meder eletronic AG, *Engen-Welschingen*

MELZER maschinenbau GmbH, *Schwelm*

MEMS Foundry, *Itzehoe*



Vacuum packaged inertial sensor on 200 mm wafer (developed and manufactured together with SensorDynamics)

Microdrop technologies GmbH, *Norderstedt*

Microelectronics Packaging, *Dresden*

Micronas GmbH, *Freiburg*

Miele & Cie., *Gütersloh*

MKS, *Munich*

Nokia Research Center, Nokia Group, *Helsinki, Finland*

NU-Tech GmbH, *Neumünster*

NXP Semiconductors, *Hamburg*

Océ-Technologies B.V., *Venlo, Netherlands*

Oerlikon AG, *Lichtenstein*

Omicron Laserage GmbH, *Rodgau*

Osram Opto Semiconductors GmbH, *Regensburg*

Oticon A/S, *Hellerup, Denmark*

PAC Tech, Packaging Technologies, *Santa Clara, USA*

Panasonic, *Neumünster*

PAV Card GmbH, *Lütjensee*

Peter Wolters GmbH, *Rendsburg*

PlanOptik AG, *Elsoff*

Plath Eft GmbH, *Norderstedt*

Polytec PT GmbH, *Waldbronn*

Preh GmbH, *Neustadt a.d.S.*

Prettl Elektronik Lübeck GmbH, *Lübeck*

Prospektiv Gesellschaft für betriebliche Zukunftsgestaltung mbH, *Dortmund*

Protec Process Systems GmbH, *Siegen*

Raytheon Anschütz GmbH, *Kiel*

Rehm Anlagenbau GmbH, *Blaubeuren-Seissen*

Reis Robotics GmbH & Co, *Obernburg*

Rena Sondermaschinen GmbH, *Gütenbach*

Robert Bosch GmbH, *Reutlingen*

Robert Bosch GmbH, *Salzgitter*

Robert Bosch GmbH, *Stuttgart*

Rutronik Elektrische Bauelemente GmbH, *Ispringen/ Pforzheim*

SAES Getters S.p.A., *Lainate/ Milan, Italy*

Sartorius Hamburg GmbH *Research & Development, Hamburg*

Sauer Danfoss Aps, *Nordborg, Denmark*

Schott AG, *Mainz*

SEF GmbH, *Scharnebek*

SensorDynamics (SD), *Lebring, Austria*

Siemens AG, *Erlangen*

Silicon Vision, *Kairo, Egypt*

SMA Regelsysteme GmbH, *Niestetal*

Smart Material GmbH, *Dresden*

SMI, *Milpitas, USA*

Smyczek, *Verl*

Sonion A/S, *Roskilde, Denmark*

Sony Deutschland GmbH, *Stuttgart*

ST Microelectronics, *Crolles, France*

ST Microelectronics Srl, *Mailand, Italy*

Still GmbH, *Hamburg*

SÜSS Microtec AG, *Garching*

Technolas GmbH, *München*

Telefonica, *Madrid, Spain*

Thales, *Paris, France*

Theon, *Athen, Greece*

Treichel Elektronik GmbH, *Springe*

Trinamic, *Hamburg*

Umicore AG & Co., *Hanau*

Vectron International GmbH & Co. KG, *Neckarbischofsheim*

Vishay BCcomponents, *Heide*

Vishay, Dimona and Holon, *Israel*

Vishay Siliconix Itzehoe GmbH, *Itzehoe*

Vishay Siliconix, *Santa Clara, USA*

Vistec, *Jena*

Volkswagen AG, *Wolfsburg*

WABCO *Fahrzeugsysteme, Hannover*

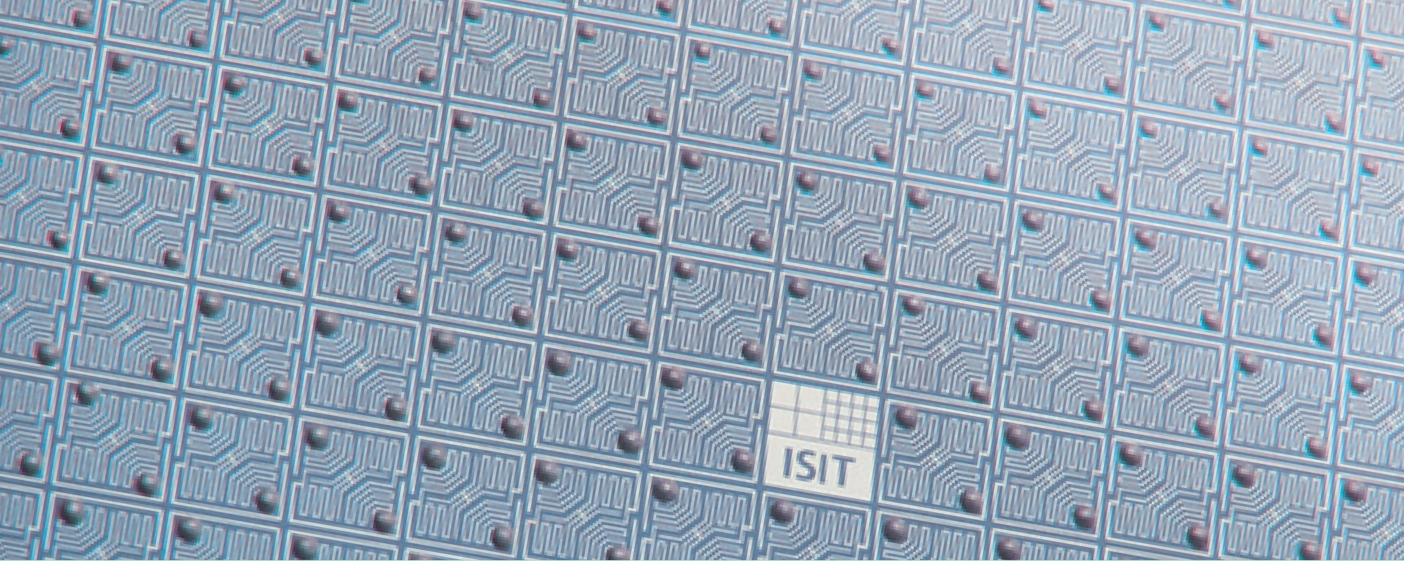
Wintershall AG, *Kassel*

Würth Elektronik GmbH, *Schopfheim*

INNOVATION CATALOGUE

ISIT offers its customers various products and services already developed for market introduction. The following table presents a summary of the essential products and services. Beyond that the utilization of patents and licences is included in the service.

Product / Service	Market	Contact Person
Testing of semiconductor manufacturing equipment	*Semiconductor equipment manufacturers*	**Dr. Gerfried Zwicker** *+ 49 (0) 4821/17-4309* *gerfried.zwicker@isit.fraunhofer.de*
Chemical-mechanical polishing (CMP), planarization	*Semiconductor device manufacturers*	**Dr. Gerfried Zwicker** *+ 49 (0) 4821/17-4309* *gerfried.zwicker@isit.fraunhofer.de*
Wafer polishing, single and double side	*Si substrates for device manufacturers*	**Dr. Gerfried Zwicker** *+ 49 (0) 4821/17-4309* *gerfried.zwicker@isit.fraunhofer.de*
IC processes and power devices CMOS, PowerMOS, IGBTs	*Semiconductor industry, IC-users*	**Detlef Friedrich** *+ 49 (0) 4821/17-4301* *detlef.friedrich@isit.fraunhofer.de*
Single processes and process module development	*Semiconductor industry, semiconductor equipment manufacturers*	**Detlef Friedrich** *+ 49 (0) 4821/17-4301* *detlef.friedrich@isit.fraunhofer.de*
Customer specific processing	*Semiconductor industry, semiconductor equipment manufacturers*	**Detlef Friedrich** *+ 49 (0) 4821/17-4301* *detlef.friedrich@isit.fraunhofer.de*
Microsystem products	*Electronic industry*	**Prof. Ralf Dudde** *+ 49 (0) 4821/17-4212* *ralf.dudde@isit.fraunhofer.de*
Inertial sensors	*Motorvehicle technology, navigation systems, measurements*	**Dr. Klaus Reimer** *+ 49 (0) 4821/17-4213* *klaus.reimer@isit.fraunhofer.de*
Piezoelectric microsystems	*Sensors and actuators*	**Hans-Joachim Quenzer** *+ 49 (0) 4821/17-4643* *hans-joachim.quenzer@isit.fraunhofer.de*
Microoptical scanners and projectors	*Biomedical technology, optical measurement industry, telecommunication*	**Ulrich Hofmann** *+ 49 (0) 4821/17-4553* *ulrich.hofmann@isit.fraunhofer.de*
Flow sensors	*Automotive, fuel cells*	**Dr. Peter Lange** *+49 (0) 4821/17-4506* *peter.lange@isit.fraunhofer.de*
Microoptical components	*Optical measurement*	**Hans-Joachim Quenzer** *+ 49 (0) 4821/17-4643* *hans-joachim.quenzer@isit.fraunhofer.de*
RF-MEMS	*Telecommunication*	**Thomas Lisec** *+ 49 (0) 4821/17-4512* *thomas.lisec@isit.fraunhofer.de*
Beam deflection components for maskless nanolithography	*Semiconductor equipment manufacturers*	**Dr. Klaus Reimer** *+ 49 (0) 4821/17-4233* *klaus.reimer@isit.fraunhofer.de*
Design and test of analogue and mixed-signal ASICs	*Measurement, automatic control industry*	**Jörg Eichholz** *+ 49 (0) 4821/17-4253* *joerg.eichholz@isit.fraunhofer.de*



Conductive adhesive applied on RFID dummy chips

Product / Service	Market	Contact Person
Design Kits	*MST foundries*	**Jörg Eichholz** *+ 49 (0) 4821/17-4253* *joerg.eichholz@isit.fraunhofer.de*
MST design and behavioral modeling	*Measurement, automatic control industry*	**Jörg Eichholz** *+ 49 (0) 4821/17-4253* *joerg.eichholz@isit.fraunhofer.de*
Electrodeposition of microstructures	*Surface micromachining*	**Martin Witt** *+ 49 (0) 4821/17-4613* *martin.witt@isit.fraunhofer.de*
Digital micromirror devices	*Communication technology*	**Dr. Klaus Reimer** *+ 49 (0) 4821/17-4233* *klaus.reimer@isit.fraunhofer.de*
Electrical biochip technology (proteins, nucleic acids, haptens)	*Biotechnology, related electronics microfluidics, environmental analysis, Si-Chipprocessing, packaging, chip loading*	**Dr. Eric Nebling** *+ 49 (0) 4821/17-4312* *eric.nebling@isit.fraunhofer.de*
Microsystem production production service	*MEMS fabless manufacturers*	**Dr. Peter Merz** *+ 49 (0) 4821/17-4221* *peter.merz@isit.fraunhofer.de*
Secondary lithium batteries based on solid state ionic conductors	*Mobile electronic equipment, medical applications, automotive, smart cards, labels, tags*	**Dr. Peter Gulde** *+49 (0) 4821/17-4307* *peter.gulde@isit.fraunhofer.de*
Battery test service, electrical parameters, climate impact, reliability, quality	*Mobile electronic equipment, medical applications, automotive, smart cards, labels, tags*	**Dr. Peter Gulde** *+49 (0) 4821/17-4307* *peter.gulde@isit.fraunhofer.de*
Quality and reliability of electronic assemblies	*Microelectronic and power electronic industry*	**Karin Pape** *+ 49 (0) 4821/17-4229* *karin.pape@isit.fraunhofer.de*
Material and damage analysis	*Microelectronic and power electronic industry*	**Helge Schimanski** *+ 49 (0) 4821/17-4639* *helge.schimanski@isit.fraunhofer.de*
Thermal measurement and simulation	*Microelectronic and power electronic industry*	**Dr. M. H. Poech** *+ 49 (0) 4821/17-4607* *max.poech@isit.fraunhofer.de*
Leadfree / RoHS transformation in electronic assembly	*Electronic industry*	**Helge Schimanski** *+49 (0) 4821/17-4639* *helge.schimanski@isit.fraunhofer.de*
Packaging for microsystems, sensors, multichip modules	*Microelectronic, sensoric and medical industry*	**Karin Pape** *+ 49 (0) 4821/17-4229* *karin.pape@isit.fraunhofer.de*
Wafer level packaging, ultra thin Si packaging and direct chip attach techniques	*Microelectronic, sensoric and medical industry, automotive industry*	**Dr. Wolfgang Reinert** *+ 49 (0) 4821/17-4617* *wolfgang.reinert@isit.fraunhofer.de*
Vacuum wafer bonding technology	*Microelectronic, sensoric and medical industry, automotive industry*	**Dr. Wolfgang Reinert** *+ 49 (0) 4821/17-4617* *wolfgang.reinert@isit.fraunhofer.de*

REPRESENTATIVE FIGURES

EXPENDITURE

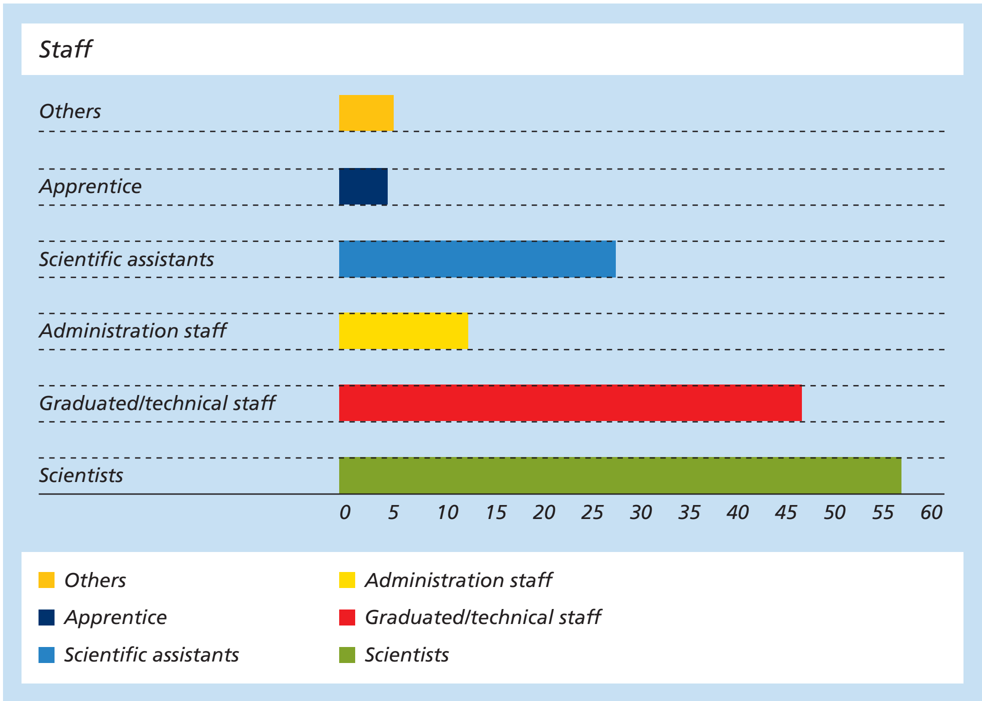
In 2009 the operating expenditure of Fraunhofer ISIT amounted to 21.306,1 T€. Salaries and wages were 7.670,8 T€, material costs and different other running costs were 12.987,8 T€. The institutional budget of capital investment was 647,5 T€.

INCOME

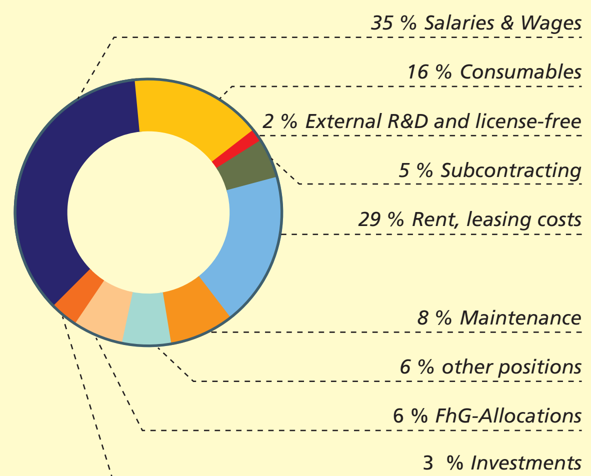
The budget was financed by proceeds of projects of industry/industrial federations/small and medium sized companies amounting to 11.575,4 T€, of government/project sponsors/federal states amounting to 3.373,5 T€ and of European Union/others amounting to 1.731,9 T€. Furthermore there were FhG-projects about 1.141,7 T€ und basic funding with 3.483,6 T€.

STAFF DEVELOPMENT

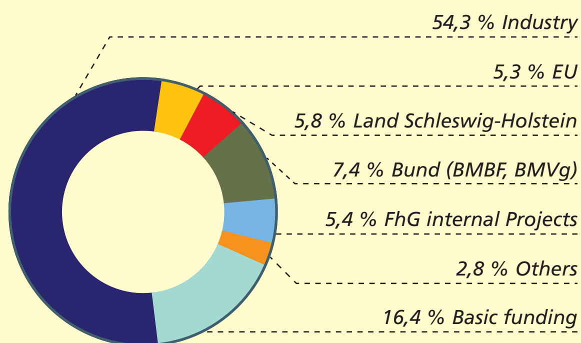
In 2009, on annual average, the staff consisted of 117 employees. 57 were employed as scientific personnel, 47 as graduated/technical personnel and 13 worked within organisation and administration. The employees were assisted through 27 scientific assistants, 5 apprentices and 6 others.

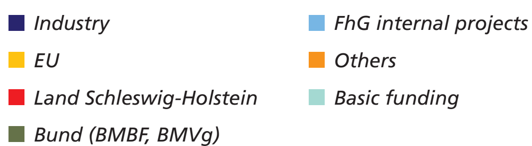


Expenditure



Income





THE FRAUNHOFER-GESELLSCHAFT

Research of practical utility lies at the heart of all activities pursued by the Fraunhofer-Gesellschaft. Founded in 1949, the research organization undertakes applied research that drives economic development and serves the wider benefit of society. Its services are solicited by customers and contractual partners in industry, the service sector and public administration.

At present, the Fraunhofer-Gesellschaft maintains more than 80 research units in Germany, including 59 Fraunhofer Institutes. The majority of the 17,000 staff are qualified scientists and engineers, who work with an annual research budget of €1.6 billion. Of this sum, more than €1.3 billion is generated through contract research. Two thirds of the Fraunhofer-Gesellschaft's contract research revenue is derived from contracts with industry and from publicly financed research projects. Only one third is contributed by the German federal and Länder governments in the form of base funding, enabling the institutes to work ahead on solutions to problems that will not become acutely relevant to industry and society until five or ten years from now.

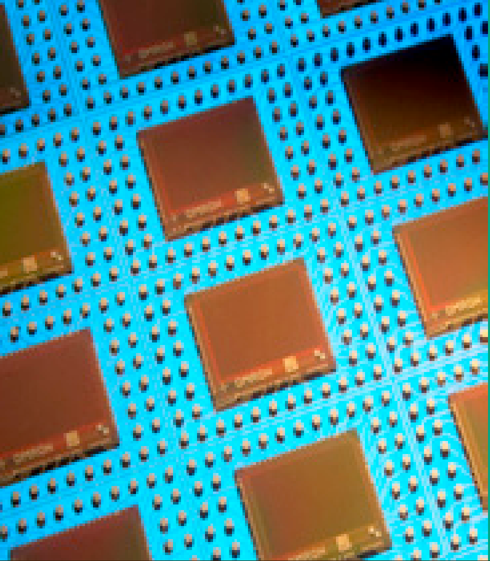
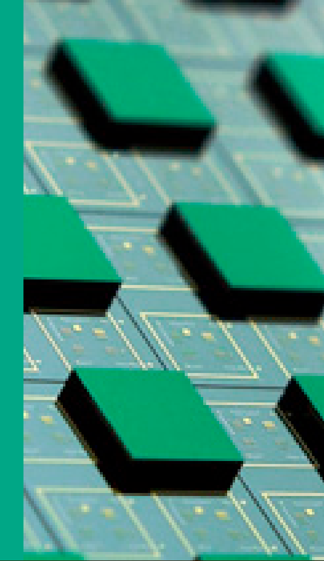
Affiliated research centers and representative offices in Europe, the USA and Asia provide contact with the regions of greatest importance to present and future scientific progress and economic development.

With its clearly defined mission of application-oriented research and its focus on key technologies of relevance to the future, the Fraunhofer-Gesellschaft plays a prominent role in the German and European innovation process. Applied research has a knock-on effect that extends beyond the direct benefits perceived by the customer: Through their research and development work, the Fraunhofer Institutes help to reinforce the competitive strength of the economy in their local region, and throughout Germany and Europe. They do so by promoting innovation, strengthening the technological base, improving the acceptance of new technologies, and helping to train the urgently needed future generation of scientists and engineers.

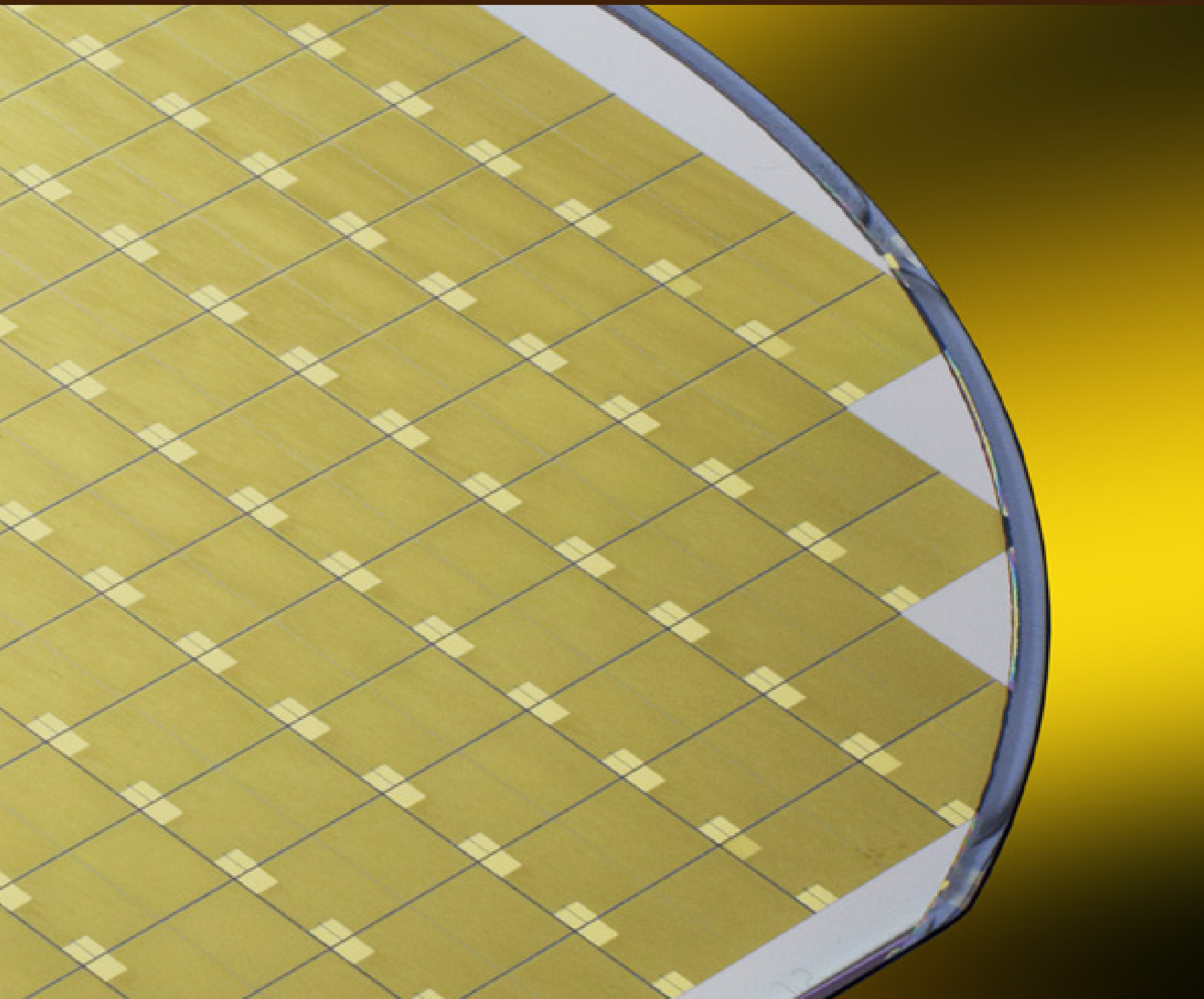
As an employer, the Fraunhofer-Gesellschaft offers its staff the opportunity to develop the professional and personal skills that will allow them to take up positions of responsibility within their institute, at universities, in industry and in society. Students who choose to work on projects at the Fraunhofer Institutes have excellent prospects of starting and developing a career in industry by virtue of the practical training and experience they have acquired.

The Fraunhofer-Gesellschaft is a recognized non-profit organization that takes its name from Joseph von Fraunhofer (1787–1826), the illustrious Munich researcher, inventor and entrepreneur.

LOCATIONS OF THE RESEARCH ESTABLISHMENT

REPRESENTATIVE RESULTS OF WORK



MICROSYSTEMS TECHNOLOGY (MEMS) AND IC DESIGN

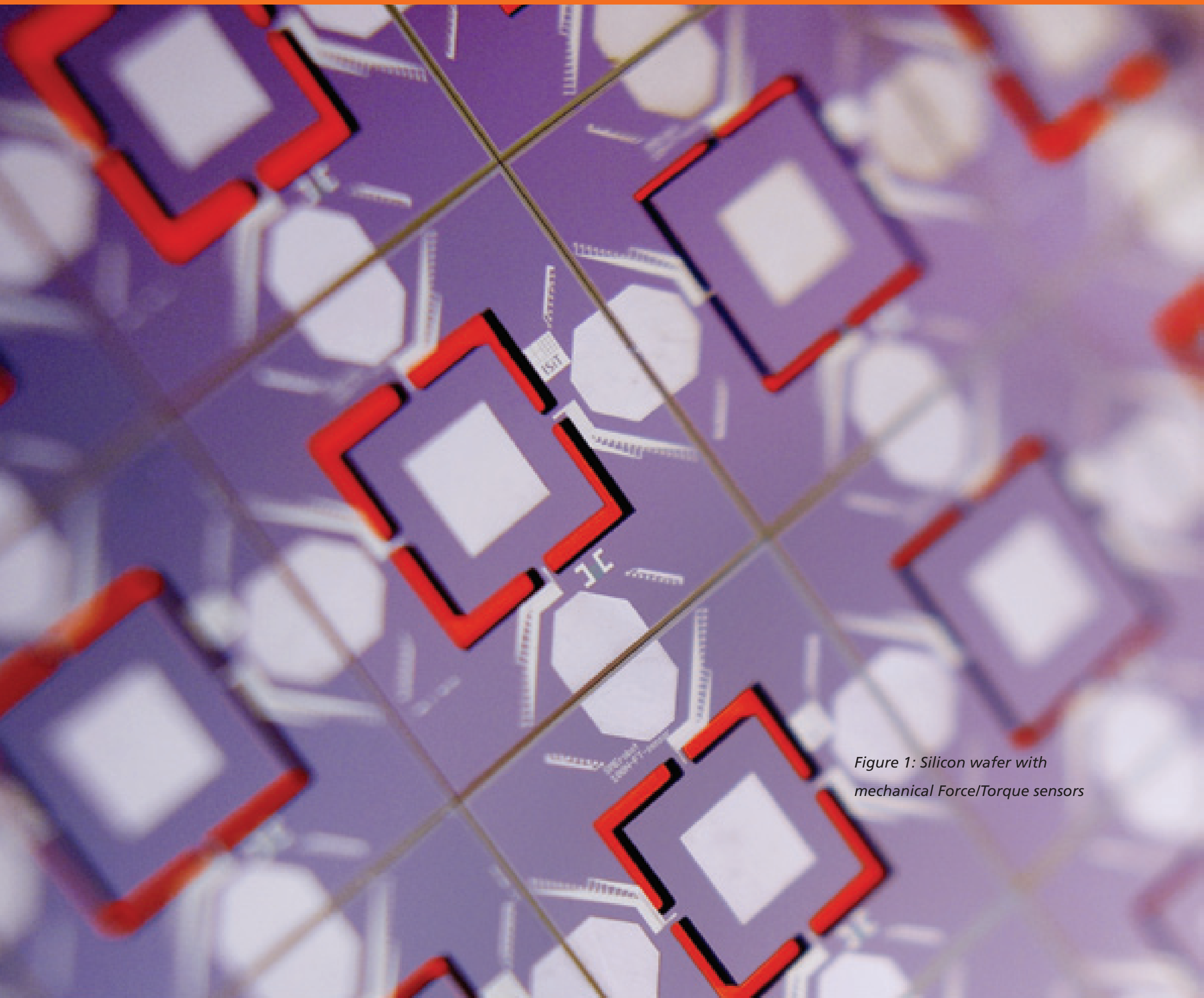


Figure 1: Silicon wafer with mechanical Force/Torque sensors

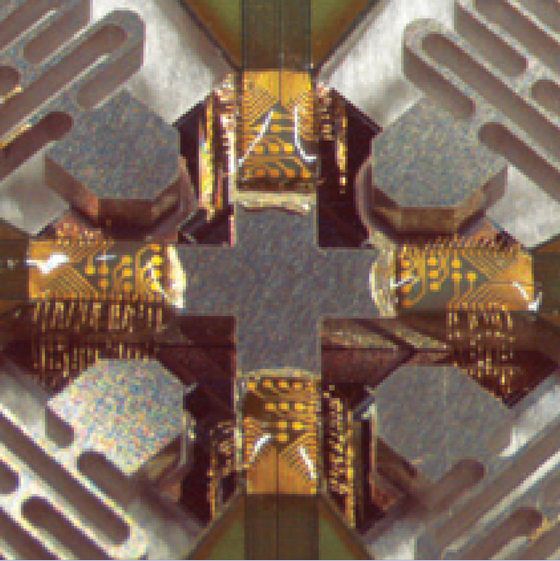


Figure 2: Transducer glued on top of a Force/Torque sensor

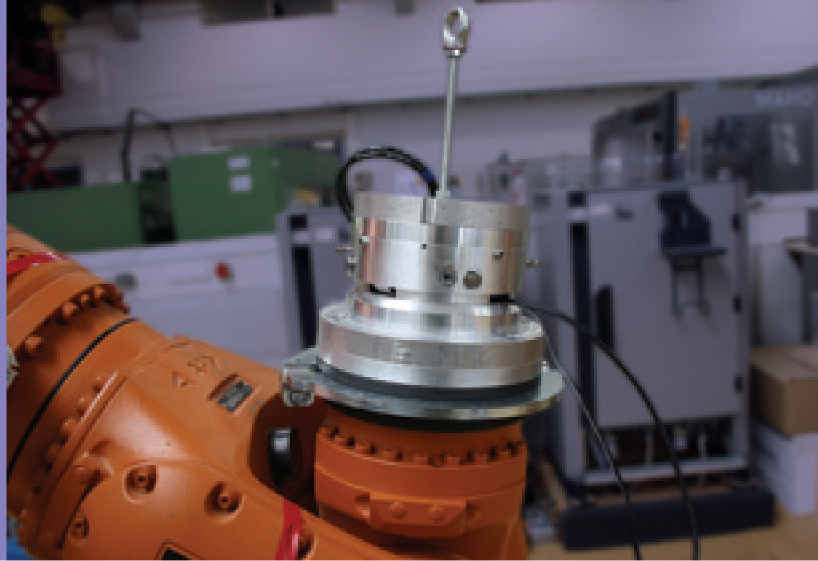


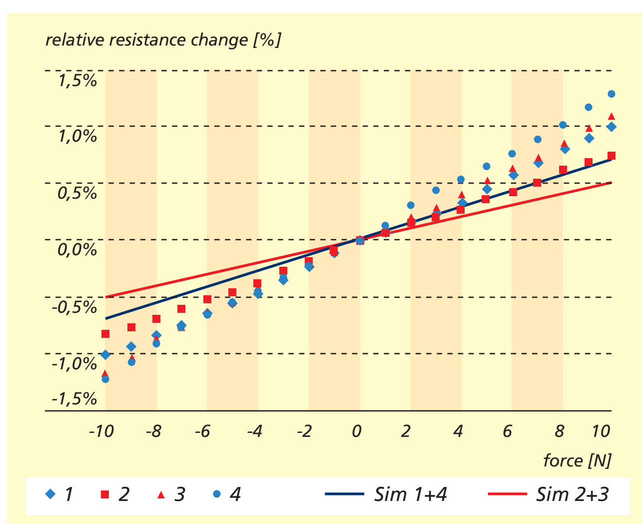
Figure 3: For lead-through programming the robot can be conducted at the bar

FORCE/TORQUE SENSOR FOR ROBOTIC INDUSTRY

Sensors, which are capable to measure forces and torques applied in all directions, are at the time rather expensive with costs beyond 2 000 € and therefore only rarely used. Since quite a lot of these force / torque sensors are needed for example in robotic applications, a low cost sensor is urgently required.

During the European project SMErobot™ (www.smerobot.org) ISIT has developed a 6 degree of freedom force / torque sensor for the robotic industry. The use of microsystem technology for this sensor allows a cost efficient mass production.

Figure 4: Measured change of resistance (dotted lines) in comparison to simulated values (solid lines)



The sensors will be manufactured using a bulk micromachining technology and will be assembled with a flat steel transducer, see figure 2. A patent was filed for the transducer that transfers the forces and torques to the silicon sensor.

To measure forces typically strain gauges are used where the electrical resistance is changed by the deformation due to the applied forces. Normally metal is used and the effect of the change of resistivity is a pure geometrical one. It was decided to take crystal silicon for force sensing instead, because of its piezo resistive property the effect $K=\Delta R/\Delta L$ is up to 50 times larger than in metals. The disadvantage is that two materials – silicon and steel – have to be connected in a safe and reliable way and due to the different coefficients of thermal expansion temperature effects are larger and have to be controlled. The measured linearity of the piezo resistors is very good, as indicated in figure 4.

Two different sensors were designed: a small one to measure forces up to 10 N and torques up 0.5 Nm and a larger one for forces up to 200 N and torques up to 10 Nm. First tests were successfully executed at a roboter for lead-through programming (see figure 3).

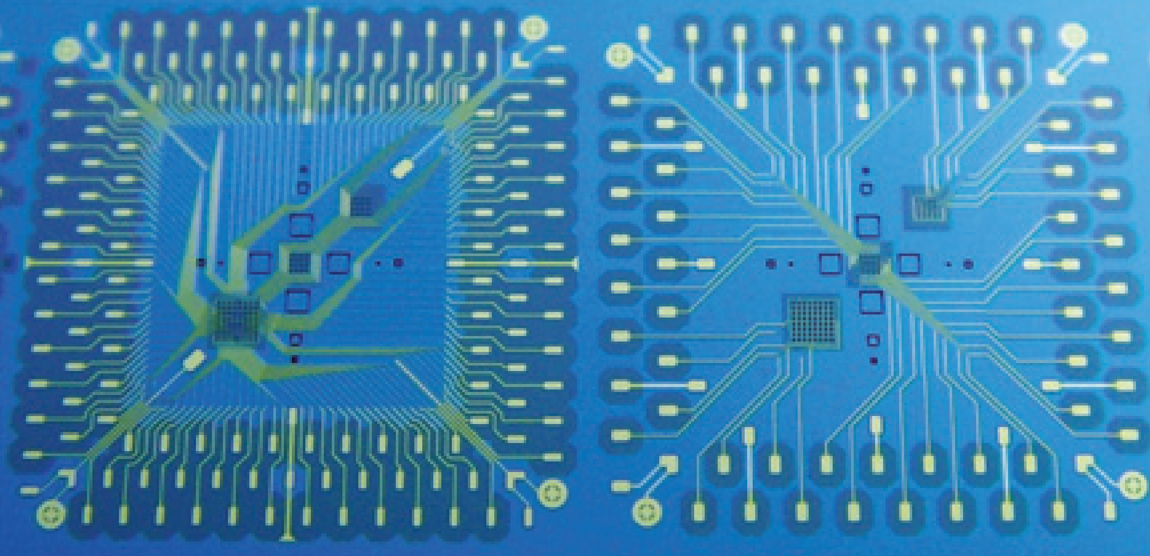


Figure 3: MDA chips with different designs realized in metal surface micromachining technology. Three areas with deflection arrays are on each chip. The full wiring can be seen.

MEMS BASED MULTI DEFLECTIONS ARRAYS FOR PARALLEL SHAPED ELECTRON BEAM LITHOGRAPHY

In today's CMOS technology the increase in integration density of semiconductor integrated circuits provides both economic and performance benefit but also implies extremely fine patterning of the features. Currently available technologies and processes will not support the complex manufacturing requirements for the 22 nm technology node and beyond. Novel approaches including new lithography equipment are urgently necessary. Even though EUV lithography is making good progress, there is still a long way to go. Especially masks for the most critical levels of a given layout in an early stage of chip-design evaluation or for fast prototyping are associated with extreme high costs. Additionally, not all semiconductor applications are high volume application.

As a general trend, the semiconductor industry is strongly driven by consumer electronic applications, which are characterized by short life cycles and a high degree of customization. This could not be realized by EUV lithography within a good cost balance. Therefore the development of a new high throughput multi-E-beam approach (Multi Shaped Beam Technology MSB) for applications in direct writing (used

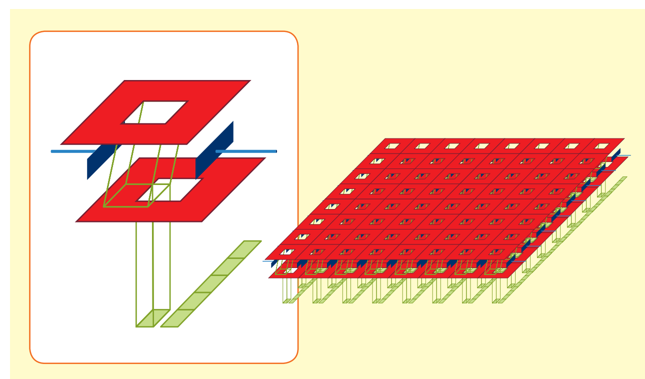


Figure 1: Conventional single Variable Shaped Beam (VSB) principle (left) and Multiple Shaped Beam (MSB) principle (right) with an array of 8 x 8 = 64 shaped beams

Table 1: Range for key specifications of Multi Deflection Arrays

Parameter	Range from …	to …
Deflector array size	8 x 8	32 x 32
Deflector pitch (µm)	60	30
Aperture size (deflector) (µm)	20	10
Si membrane thickness (µm)	100	100
Deflector height (µm)	100	50
Geometric shape deviation (µm) (deflector electrodes)	< ± 0.2	< ± 0.2
Deflector wiring resistance (Ohm)	< 500	< 500
Placement accuracy, apertures vs. deflectors (nm)	< 250	< 150

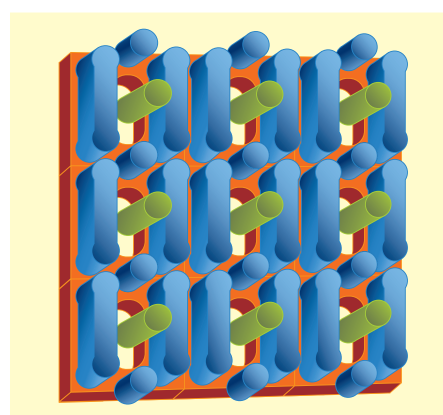


Figure 2: Electrode design for a 60 µm MDA cell

Figure 4: Deflection array realized in metal surface micromachining technology

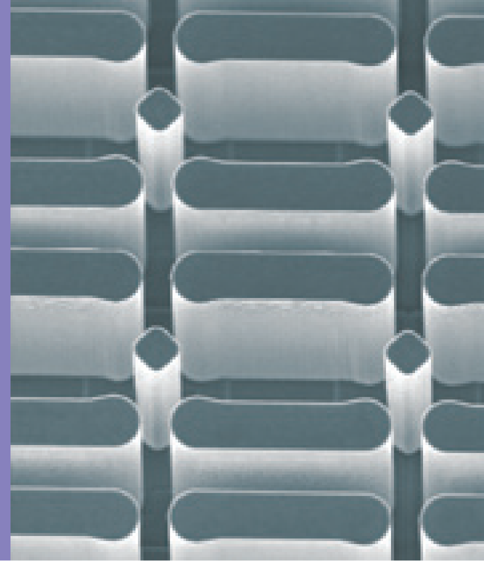


Figure 5: Deflection array realized in polysilicon surface micromachining technology

Technology	metal surface micromachining	polysilicon surface micromachining
Main Characteristic	- Thick resist technology - Electroplating process - Gold wiring	- EpiPoly deposition - DRIE structuring - Buried poly wiring
Advantage	Wiring conductance	Shape accuracy
Weakness	Shape accuracy	Wiring conductance

Table 2: Comparison of metal surface micromachining technology and the polysilicon surface micromachining technology

in mix-and-match technique with optical 193 nm lithography) as well as mask writing is of major interest for future ASIC development.

The company VISTEC Electron Beam (former LEICA Microsystems Lithography) proposed a Multiple Shaped Beam (MSB) technology concept, which is drastically different from previous presented Projection Maskless Lithography technologies. Instead of creating ten thousands of „electron beam pixels" by an aperture plate array which are switched on and off to write a given pattern on the substrate (see Fraunhofer ISIT annual report 2004/p. 42 and 2008/p. 44), the MSB technology forms variable „electron beam shapes" analogously to the proven and mature variable shaped single beam technology but using an array of multiple beamlets, which are individually controllable in its x- and y-shape size and its beam-ontime (see figure 1). The development of the MSB technology which applies in parallel multiple shaped electron beams will remarkably improve the throughput of E-beam lithography. For mask writing, a write time advantage of 10x – 50x and more can be expected from the MSB tool depending on the MSB array size and the kind of pattern.

One of the key components of the MSB technology is a MEMS based deflector array as it is shown in principle in figure 2. The red area is the base plate of the array with apertures for the electron beam and the blue structures are representing the deflection and compensation electrodes. The electron beam is drawn in green. MSB technology requires low aberration deflection and therefore challenging accuracy of the applied process technology. A range for some key specifications for multi deflection arrays (MDA) are summarized in table 1.

Fraunhofer ISIT has two technologies available which are expected to fulfil the above described requirements: the metal surface micromachining technology and the polysilicon surface micromachining technology. So a common project between VISTEC and ISIT has been defined to evaluate the performance of both processes with respect to the specifications of Multi Deflection Arrays (MDAs).

The metal surface micromachining technology is an alternative way to build up complete MEMS systems. By using mainly electroplating and lithography in combination with PVD, PECVD and etching processes it is possible to fit

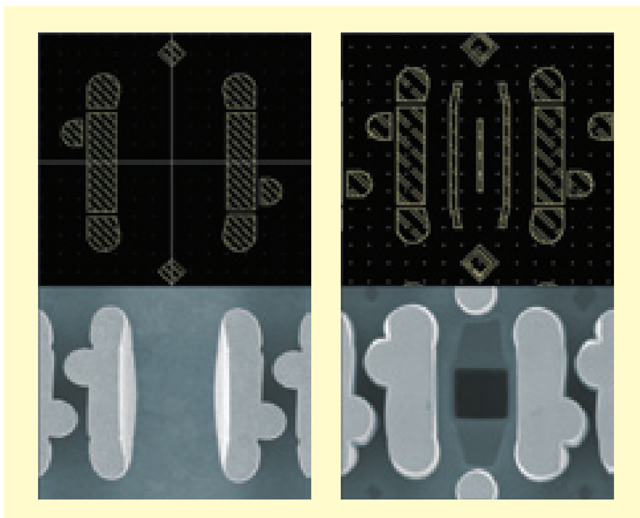


Figure 6: Deflection array realized in metal surface micromachining technology

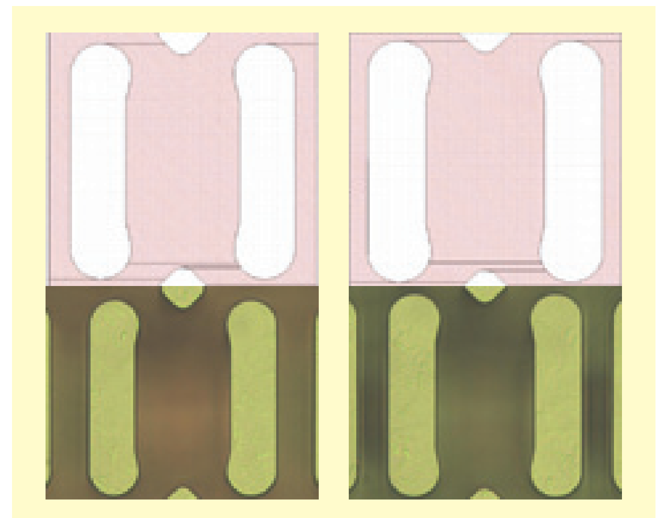


Figure 7: Deflection array realized in polysilicon surface micromachining technology

the requirements for a variety of MEMS applications. The low (CMOS compatible) temperature budget of the whole process makes it suitable for the monolithical integration of a complete MEMS system. Additional a high flexibility in design and thickness is given. The advantages and weaknesses of this processes are addressed in table 2.

The polysilicon surface micromachining technology features a low stress poly silicon layer for the realisation of mechanical active and passive MEMS structures with thicknesses upto 100 µm. The use of high resolution lithography allows minimal structure dimension and high shape accuracy. An additional electrode layer between the polysilicon layer and the base wafer is implemented. The advantages and weaknesses of this process are addressed in table 2.

During the project a lot of Multi Deflection Array designs have been processed with 16 to 64 deflection units per array and different wiring strategies. Figure 3 shows two design examples (here in metal surface micromachining technology) with a completely wired 4x 4 array (right side) and a completely wired 8x 8 array (left side). In both technologies full functional Multi Deflection Array chips has been fabricated and chracterized. Both technologies were able to reach in a first step a deflector height of about 60 µm. With some further development effort the required 100 µm deflector height seemed to be

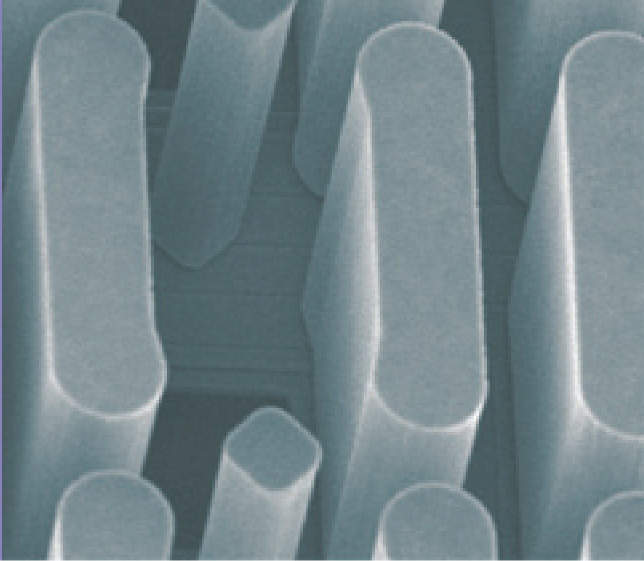


Figure 8: View inside a deflection array realized with polysilicon surface micromachining technology

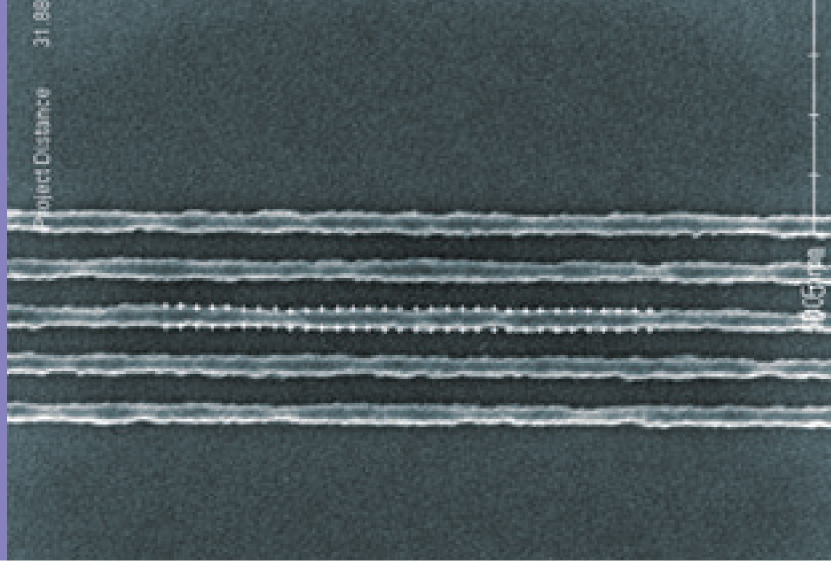


Figure 9: First result of parallel shaped electron beam lithography using ISIT fabricated Multi Deflection Array (Lines and spaces in resist, design pitch = 80 nm, design line = 30 nm, measured line = 32 nm)

possible. As expected the wiring resistance from deflector to an outer conatact pad is for the metal surface micromachining technology in the range of some Ohms, but for polysilicon surface micromachining technology in the range of about 1000 Ohms. If this difference has already influence on the functionality could only be judged by test within the electron optical column. In both technologies the complex wiring could be realized without shorts. Overview of these data are listed in table 3. The geometric shape accuracy is excellent with the polysilicon surface micromachining technology (figures 5, 7) and good with metal surface micromachining technology (figures 4, 6) after improvement by introducing subresolution compensation structures during the thick resist lithography process. The placement accuracy between aperture and deflectors is within the required value of 250 nm for the first phase, demonstrated on figure 8. Complete processed chips fabricated in both technologies were sent to the project partner VISTEC, who built these chips in the electron optical column of an available e-beam writing tool. VISTEC performed sub 100 nm e-beam writing experiments in the multi beam mode applying the ISIT MDA chips and results in first 30 nm structures shown in figure 9. Further tests are in preparation at VISTEC to evaluate differences in behavior of the MDAs, fabricated in the two technologies, concerning position precision in deflection, timing precision in deflection, charging and longterm stability.

Table 3: Achieved results applying both technologies for fabrication of Multi Deflections Arrays

	Technology	
Achieved results	metal surface micromachining	polysilicon surface micromachining
Deflector height (µm)	55	65
Deflector wiring resistance (Ohm)	approx. 3	approx. 1200
Shorts in wiring	non	non

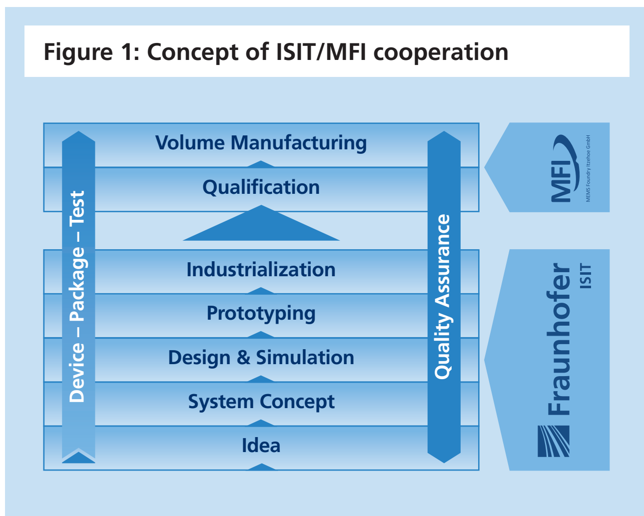
MEMS cleanroom production

MEMS FOUNDRY ITZEHOE GMBH

MFI was established in 2009 as a spin-off from the Fraunhofer ISIT and is active within the same wafer fabrication facility in Itzehoe. The MEMS Foundry Itzehoe GmbH (MFI) is focusing on MEMS production services and acts as a customer oriented contract manufacturer. Customer specific MEMS devices like micro sensors, actors, micro optical structures, functional cap wafers and hermetic wafer level packaging processes are in the scope of the foundry business. The service offer aims at shortening the time to market of customer specific developments but also accelerates the exploitation and commercialization of existing and emerging technologies, applications and intellectual property.

The management team of MFI evolved from the Fraunhofer ISIT MEMS group and has outstanding experience and skills within the industrial development, industrialization and production of MEMS devices and components for automotive and other markets.

Figure 1: Concept of ISIT/MFI cooperation



One-Stop-Shop for MEMS

A close contracted cooperation between Fraunhofer ISIT and MFI is originating a successful and sustained MEMS product development. Here Fraunhofer ISIT brings in its longtime know-how for the design, technology development and prototyping of new MEMS devices. MFI is monitoring and supporting the product industrialization phase and manages the ramp up to volume production. Together with Fraunhofer ISIT MFI can offer a complete one-stop-shop for MEMS products which includes all stages of a product cycle from the basic idea up to sustainable high volume production.

MEMS Technology and Service

MFI provides an unprecedented broad MEMS technology landscape. Next to standard MEMS processing MFI features a profound silicon and thick layer epi-silicon based surface micromachining technology. The implementation of various process modules based on different ceramic and metallic materials opens up the realization of multiple MEMS architectures. For actuators different piezoelectric materials like PZT and AlN are available. Wafer Level Packaging is the key technology for cost-efficient peripheral functionality like mechanical protection, hermetic housing or added optical system elements. MFI has excellent knowledge and capabilities to provide the optimum package solution on wafer scale for each MEMS application effecting in reduced device size, low production costs and high reliability at superior performance. Finally different Through Silicon Vias (TSV) technologies are completing modules to a seamless integrated MEMS process flow.
The MEMS production is based on a fully equipped class 10 MEMS clean room with a floor space of 1000 m^2. The wafer substrate size is 8 inch making the products also commercially attractive for low cost consumer application. For wafer

Process control at HF vapour phase etch

finalisation a class 10.000 back end is available. The whole production control is steered and controlled by an automated manufacturing execution software which includes also automated data acquisition and analysis for statistical process control (SPC). A highly qualified and motivated operating personal secures a stable and continuous production flow. MFI has extensive experience in process industrialisation and transfer from prototype phase to volume production according to VDA 6.3 and ISO/TS 16949. Especially the implementation of SPC methods, continuous process improvement and yield management and the use of quality management tools like FMEA, control plan, control chart, fishbone diagram are among the core competences of MFI. We support customers from the beginning by providing efficient cost projection and controlling.

Figure 2: MEMS Technology Landscape

Lithography
- 0,8 µm Widefield Stepper, Proximity Exposure
- Front-to-Backside Alignment
- Spin Coating, Spray Coating
- Positive, Negative Dry Film, Thick Resist

Wafer Level Packaging
- Eutectic, Solder Alloy, Anodic Bonding
- Glass Frit, Fusion Bonding
- High Capacity Getter Films for Vacuum WLP
- Optical WLP, Glass Micromachining

Film Deposition
- SiO_2 and LPCVD Si_3N_4
- PECVD SiO_2 and Si_3N_4, a-Si, up to 550 °C
- Thick Epi Poly Silicon (10 – 100 µm), SiGe
- Piezoelectric Layers: AlN, PZT
- Sputter Metal: Al, Mo, Ti, TiN, Cr, Au, Ta, Cu
- Evaporation Metal: Ti, Ta, Au, Pt, Ir, Ag
- Electroplating: Au, Sn, Cu, Ni

Etching
- RIE: Si, SiO_2, SiN, AlN, PZT
- DRIE: High Precision, High Rate
- Wet Etch: Si, SiO_2, SiN
- Metal Etch: Al, Cu, Au, Cr, Ti, Mo
- Al-compatible anisotropic Si-Etch
- Single Wafer Spin Etching: Cu, Au, Ti, SiO_2
- Vapour Phase Etch: HF, XeF_2

Surface Functionality
- Chemical Mechanical Polishing
- Organic and Anorganic Anti-Stiction Coatings
- Surface Hardening
- Anti Reflective Coatings

Postprocessing & Analysis
- Dicing, Grinding, DBG, Wafertest
- Reliability Device Qualification (AEC-Q100)
- Shock&Vibration, High-g CA, Fatigue Testing
- Failure Analysis, SEM, XRay, SAM, …

MFI in Short
- Premium 8-Inch Wafer Line
- Manufacturing Execution System (MES) with Integrated SPC
- 1000 m^2 Volume Production Clean Room Facility
- Metrology for Process Control, SPC and Cpk
- R&D Cooperation with ISIT MEMS, IC and Packaging Group

Nanolab lithograpy area

THE KIEL NANO LABORATORY

A strategic objective of Fraunhofer ISIT is to strengthen its partnerships with research institutions in Schleswig-Holstein and Hamburg. In this context the most important partner certainly is the Christian-Albrechts University in Kiel (CAU), especially the Faculty of Engineering.
A personnel linkage of ISIT and CAU has already been established by the professorial appointments of ISIT director Prof. Wolfgang Benecke, chair for "Technologies of Silicon based Micro- and Nanosystems" at the Institute for Electrical and Information Engineering and ISIT deputy director Prof. Bernhard Wagner, chair for "Materials and Processes for Nanosystem Technologies" at the Institute for Material Science.

In the field of Micro-Nanosystems ISIT and CAU complement each other ideally in the value chain of basic research and application development. At University of Kiel the focus is on the investigation of new processes for nanostructures and functional materials while ISIT is concentrating on the process integration and manufacturability of complete microcomponents and -systems. Mid 2009 Prof. Benecke and Prof. Wagner have started to establish a joint research group at University of Kiel, headed by Dr. Stephan Warnat. The major objective of this group is to prepare new strategic fields for ISIT by an intensive knowledge exchange and cooperation with research groups at CAU. Also very important is to inspire and educate students on new technologies and research topics and to accomplish master and PhD theses.

The Faculty of Engineering in Kiel operates a very well equipped clean room facility for research and development in Micro-Nanotechnologies, the "Kiel Nano Laboratory". This new research facility has opened in 2008, funded by Schleswig-Holstein and the European Commission. Figure 1 shows a floor plan of the nano-laboratory. The lab was planned and built by Prof. Eckhard Quandt, chair for "Inorganic Functional Materials", supported by Dr. Eike Krullmann from ISIT. The major part of the laboratory is occupied by a clean room with an area of about 300 m^2 and a class of 100 to 1000. In addition services on material characterization can be offered utilizing an advanced high-resolution transmission electron microscope (HRTEM). The clean room is equipped with a variety of tools for 6"-wafer processing as UV-, nanoimprint- and e-beam lithography, PECVD, wet and dry etching, electroplating and especially several sputtering equipments. Fig. 2 shows a view of the lithography area.

It is planned that the first activities of the ISIT group at CAU will concentrate on the development of piezoelectric and magnetoelectric thin film materials, in part supported by the SFB 855 which is dedicated to research on biomagnetic sensing. Further research will also focus on new materials for energy conversion and storage.

MICROSYSTEMS TECHNOLOGY (MEMS) AND IC DESIGN

Nanolab sputtering area

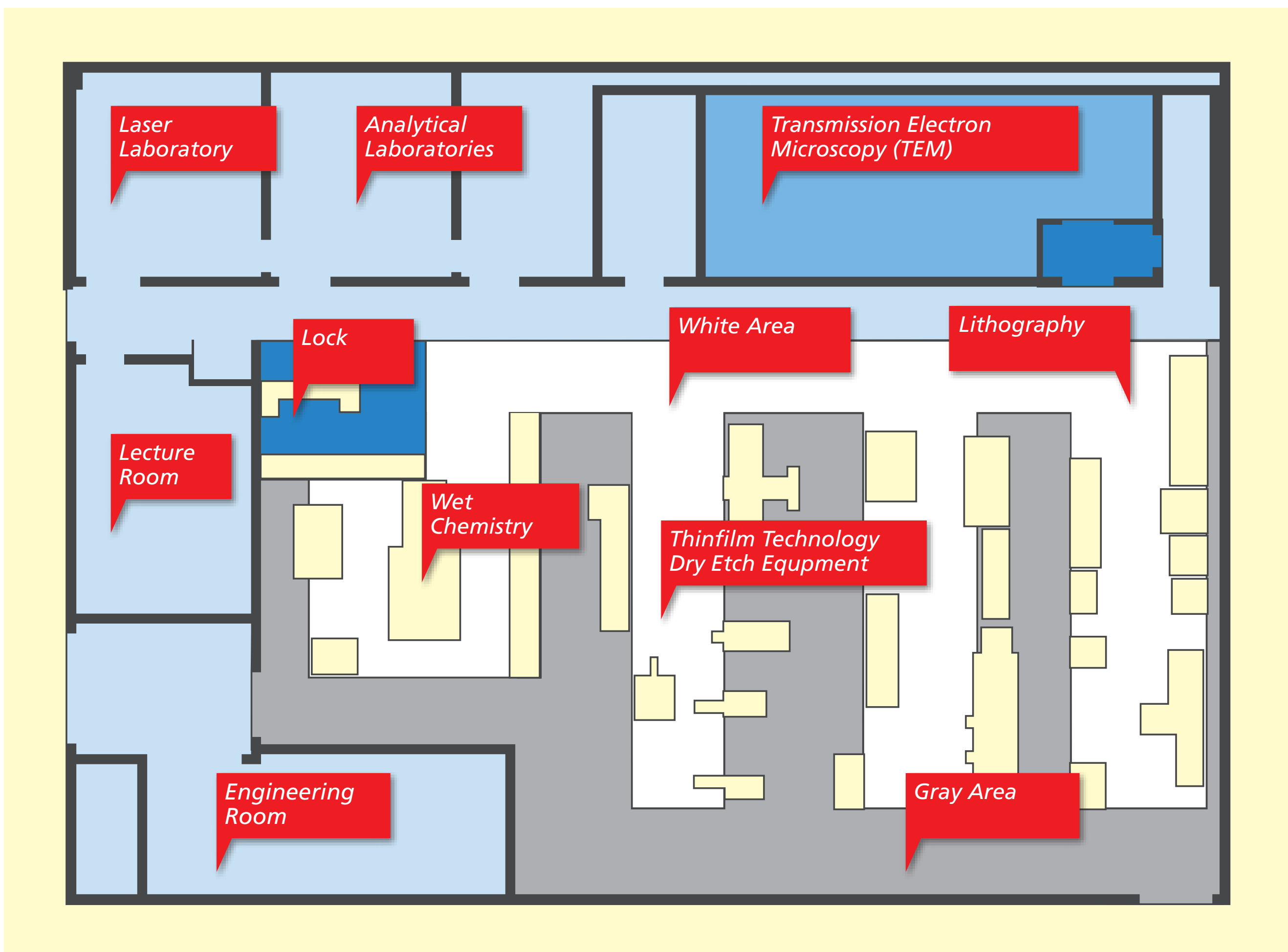
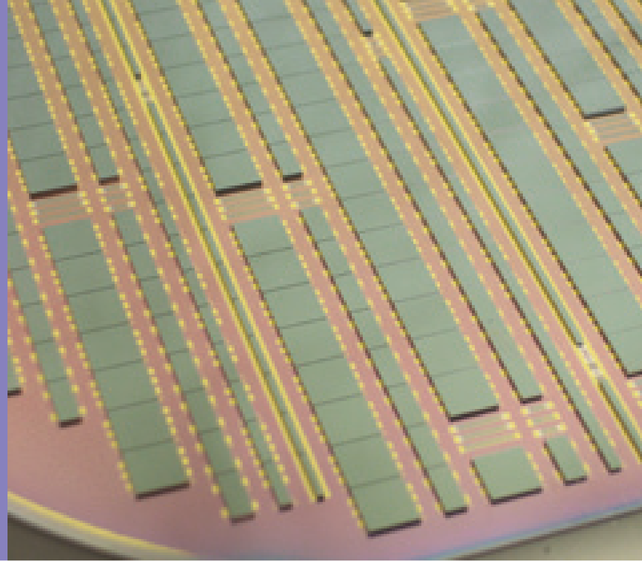


Figure 1: Floorplan of the Kiel nanolaboratory



Test packages for RF applications

MEMSPACK – ZERO- AND FIRST-LEVEL PACKAGING OF RF-MEMS

Today, the commercialization of RF-MEMS, is greatly affected by two critical factors, the related developing of an appropriate packaging technology and solving the reliability issues. Since the MEMSPACK project tackles the packaging issue, the project's main objective is to (further) develop and to characterize generic wafer-level (or 0-level) & 1-level packaging solutions for housing RF-MEMS components and systems. Examples of possible packages that are studied in the MEMSPACK project include (see figure 1):

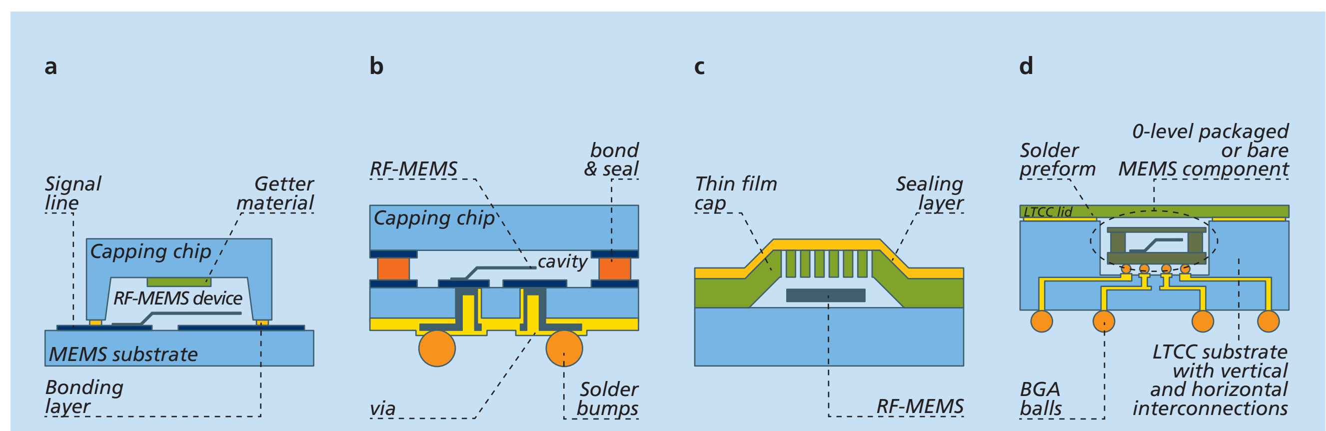
- (a) 0-level chip-capping with horizontal planar feedthroughs
- (b) 0-level chip capping with vertical (through wafer via) feedthroughs
- (c) 0-level thin-film capping
- (d) 1-level packaging based on LTCC.

The project addresses all relevant issues, starting with the design of the package (including RF design, thermomechanical design, design for reliability), the packaging technology (e.g., 0-level "chip capping" technology, 0-level "thin film capping", 1-level packaging technology), up to the package characterization (RF, temperature stability, hermeticity) and the package evaluation (impact of the package on the device performance, towards meeting industrial specifications). One of the expected outcomes of the project will be an RF-MEMS packaging design guideline, that can effectively be used by industry for the development and exploitation of RF-MEMS. The MEMSPACK consortium is supported from its Industrial Advisory Board (IAB).

The project partners are:

- IMEC (Belgium): coordinator,
  0-level packaging technology supplier
- VTT (Finland): 1-level packaging technology supplier
- Fraunhofer ISIT (Germany):
  0-level packaging technology supplier
- University of Perugia (Italy):
  RF design and characterization of the package
- FBK-irst (Italy): supplier of (RF-MEMS) test vehicles to characterize the package

Figure 1: Illustration of different packaging concepts for RF-MEMS



- CNRS-IEMN (France): RF design and test, 0-level packaging technology supplier
- MEMS TC (The Netherlands): thermomechanical design and modeling, and interface to the Industrial Advisory Board

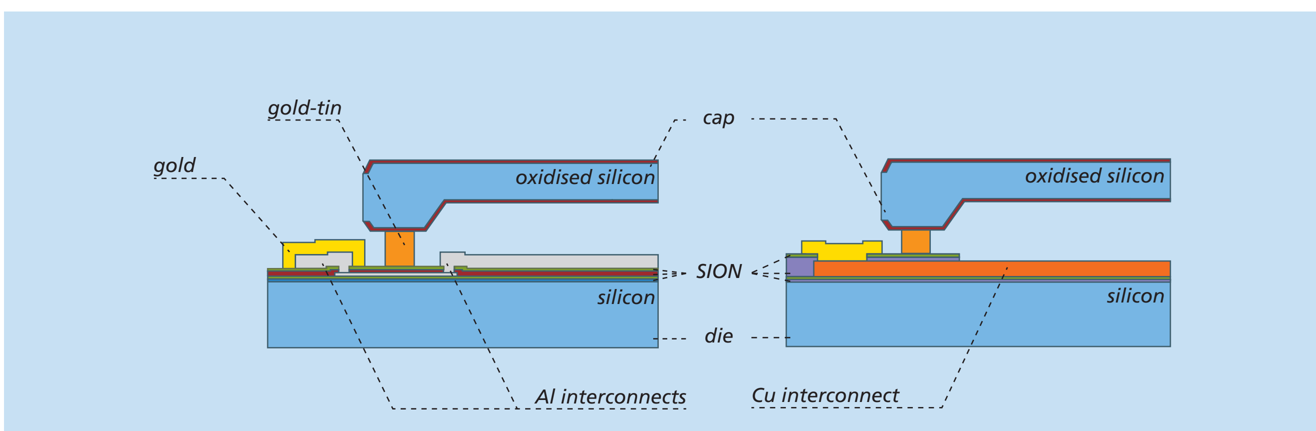
The project has started June 1, 2008 and the planned duration is 3 years.

The main work of Fraunhofer ISIT in MEMSPACK is focused on the development of a suitable wafer-level capping process using lateral RF-feedthroughs through the bond frame. MEMS and CAP wafers are made from high resistivity silicon, while the assembly is done by wafer bonding using a metal soldering process. The initial sealing rings are formed by electroplating of AuSn stack. This baseline technology is already available and is developed further on in this project.
A CPW (coplanar waveguide) line on MEMS wafer is used to achieve a 50 Ω transmission line. Two process versions were realized.

In a first concept thin buried aluminium feedthroughs are used as an underpath in the bond frame while the remain CPW lines are realized by 3 µm thick Al layer (see figure 2 left).
In addition, outside the cavity the thick Al is reinforced with electroplated gold to avoid corrosion. The isolation between sealing ring and feedthrough is formed by a stack of Si-Oxide and Si-Nitride films.

In a second concept a planar copper feedthrough is used instead of aluminium, see figure 2 right. Both RF feedthroughs and transmission lines are made from thick Copper patterned by CMP (chemical mechanical polishing). The advantage of the so called damascene technology is that due to the polished copper surface nearly no topography must be leveled by the sealing ring alloy of the bond frame. Moreover the continuous thick copper interconnects in this concept provides a more conductive feedthrough than the first version. Therefore it is expected to achieve a better RF-performance. Like in the first concept the lines outside the cavity are reinforced with Au to

Figure 2: Sketches of the RF-MEMS packaging technology. Left: based on aluminium thin film buried RF feedthroughs. Right: based on plated copper planarized RF feedthroughs



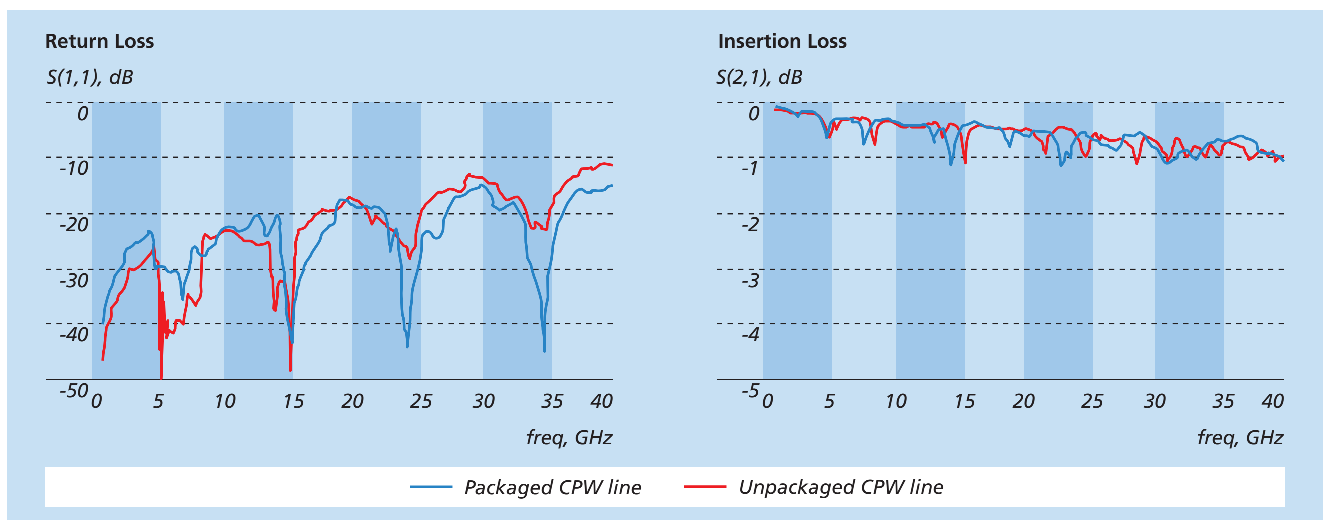


Figure 3: Measured return loss and insertion loss for unpackaged and packaged CPW line

protect the Cu against corrosion. In both concepts a 60 µm deep cavity is used in the cap wafer to avoid an interference of the Silicon of the cap wafer within CPW line.

To study the influence on the performance three different sealing ring widths are realized (50 µm, 100 µm, 200 µm). A small ring width is preferred from RF point of view since it helps minimizing the capacitive coupling of the RF signal with the sealing ring which is strictly depending on the overlapping area between the RF line and the ring.

The measured results are in a good agreement with the simulation. An significant improvement of RF performance in term of return and insertion loss is observed with compensated bond frame crossing (return loss better than 15dB and insertion loss better than 0,2 dB/mm up to 30 GHz).

The measured losses are summarized in figure 3. A silicon cap with 60 µm cavity has no significant impact on the CPW characteristics.

In the project the different packaging concepts are evaluated with respect to aspects like:

- Hermeticity for moisture;
- Hermeticity for gasses;
- Mechanical Stress/ Strain;
- RF Performance (losses);
- Mechanical strength of the package;
- Temperature on die;
- Power handling;
- ESD sensitivity.

Target parameters are defined for the manufactured samples at ISIT and are listed up in the following table 1.

The manufacturing of the first samples is meanwhile finished and the testing of the packaging performance is actually started. A second run is foreseen in the project to optimize the design and process.

Baseline Spec	Target Parameters
Packaging concept	0-level packaging
Packaging technology	Eutectic bonding
Bondframe width	20-100 µm
Bond frame material	Au/Sn
Processing temperature	< 300°C
Max. survive temperature	> 300°C
Feedthrough	Horizontal, burried, planar without topography
Hermeticity	Very good
Leake rate	10E-15 mbar.l /sec
Min. cavity pressure	1 mbar, 10E-4 mbar (with getter)
Cavity atmosphere	Inert gas
Mechan. stability	Good
Total thickness of device	< 700 µm
Transition lines	CPW / (micro strip)
Transition lines material	Thick Al, thick copper
RF operating range	Up to 70 GHz
Max insertion loss	< 0.2 dB@6GHz
Max. return loss	< 30dB@6GHz
Cap material	High res. Silicon
Cavity height	60 µm
Max. hydrostatic load	1 bar
Accuracy bonding alignment	10 µm

Table 1: Boundary conditions of the packaging concepts from ISIT according to MEMSPACK baseline specifications

EQUIPMENT MODERNISATION, TRANSFER TO 8 INCH PRODUCTION TECHNOLOGY

In Itzehoe ISIT is running a microelectronic pilot production line since 1995. For development of advanced industrial production processes ISIT has to run state of the art equipments and semiconductor processes.
Therefore in 2009 the project „Center of Competence for large wafer diameters“ was started to shift all processes to 8 inch (200 mm) wafer diameter production technology. This major modernisation programme was coordinated with the co-operation partner Vishay who has implemented an 8 inch production technology for its MOSFET production, too.

For set-up of new equipment in Itzehoe and upgrade of existing equipments in total 10,4 Mio.€ have been invested. This large investment project was financed by the ministry of economic affairs Schleswig-Holstein as part of the „Zukunftsprogramm Wirtschaft“. A quarter of the investment costs were co financed by Fraunhofer central administration. While the 8“-transfer for power electronics development was implemented by ISIT in recent years the last investments were mainly arranged for microsystem (MEMS) special processes in the backend (MTK) area.
For development of new sensing and actuating microstructures often new and non-standardized materials have to be used. Therefore several special equipments had to be ordered that do not operate according to microelectronics production technologies. As an example in the backend area electroplating processes are utilised or glas wafers are processed.

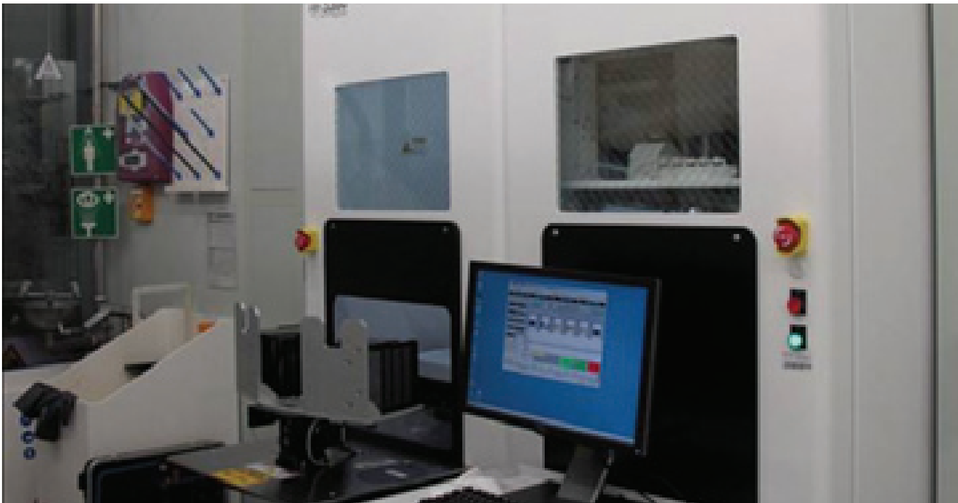
Beginning 2010 ISIT will have transferred all processes to 8 inch including the microsystem special processes. With this modernisation programme ISIT is in line with worldwide advanced MEMS process technologies that are migrating to 8 inch technologies due to increasing cost pressure for MEMS products. Bosch has set-up in Reutlingen a new 8 inch Fab that will also be used for MEMS sensor production, Freescale has converted an 8 inch line in Austin, Texas to MEMS production and STMicroelectronics is producing MEMS devices with an 8 inch line in Italy.
The main challenge in converting to larger wafer diameters is the transfer of critical processes with sufficient parameter control and quality. Since MEMS makes often use of non-standard processes this transfer necessitates a high commitment of development effort.
The following main equipments have been procured:

Equipment	Producer
Low Pressure Epitaxial Reactor	ASM
Metal Sputter Tool	Oerlikon
PZT Sputter Chamber	Oerlikon
Metal Spray Etcher	SSEC
PECVD	Applied Materials
Deep Reactive Ion Etcher	STS
Silicon Sacrifical Layer Etch	Memsstar
Optical Wafer Inspection Tool	Rudolph
Test and Measurement Tools	Miscellaneous
8“ upgrade sets	Miscellaneous

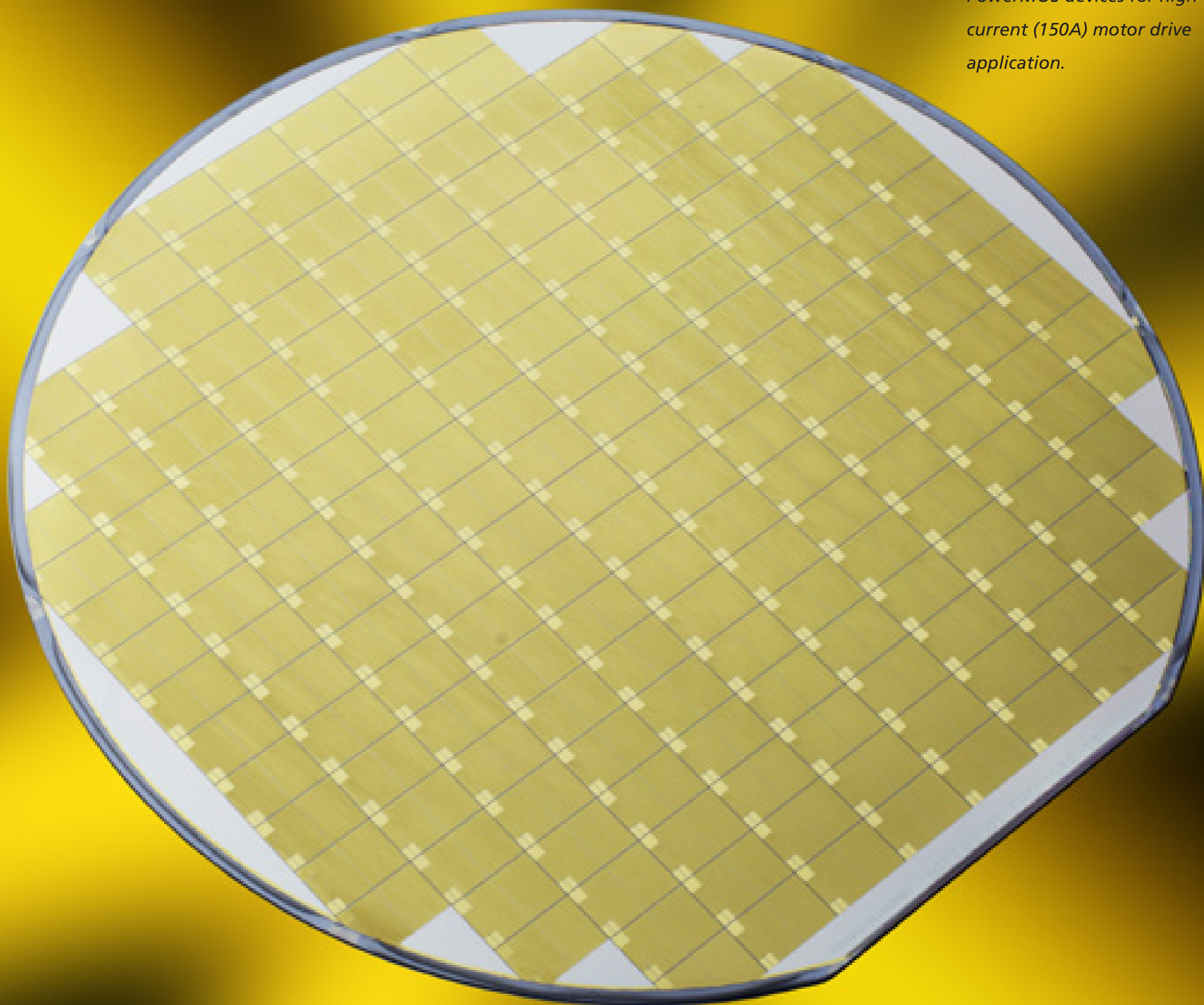
Most equipments have been installed in 2009. The installations were co-ordinated with Vishay, some installation processes were done or supervised by Vishay on behalf of ISIT. In spring 2010 all processes will be transferred to 8 inch technology and 200mm wafers will be the working standard within ISIT. Figure 1 and 2 show exemplarily two new installed equipments.

Figure 1: STS VPX cluster platform with STS Pegasus deep reactive ion etcher (cleanroom view and greyroom view)
Typical parameter: Etchrate: > 40 µm/min; aspect ratio: Holes > 25:1; Trenches > 50:1; Selectivity: Si:Photoresist>150:1; Si:SiO2>250:1

Figure 2: SSEC model 3303 single wafer etch & clean processor for metal wet etch (cleanroom view, etch chamber and disposal module)
Typical parameter: Chamber 1: Gold etching; Chamber 2: Titanium etching; SC1 cleaning; Chamber 3: Copper etching; Optical endpoint detection



IC TECHNOLOGY AND POWER ELECTRONICS



Wafer with customer specific PowerMOS devices for high current (150A) motor drive application.

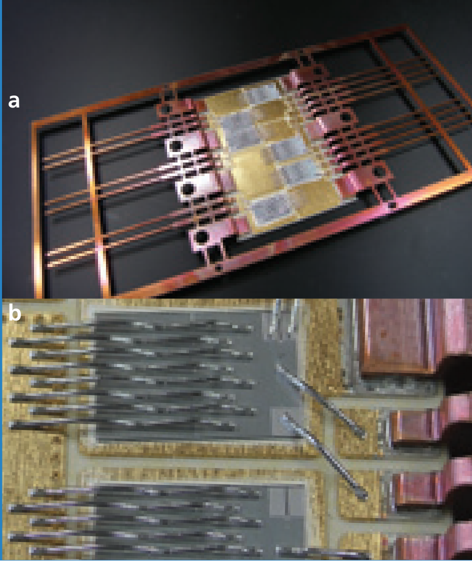


Figure 1: PowerMOS devices mounted by Ag sintering on a leadframe with DCB (a: overview, b: detail)

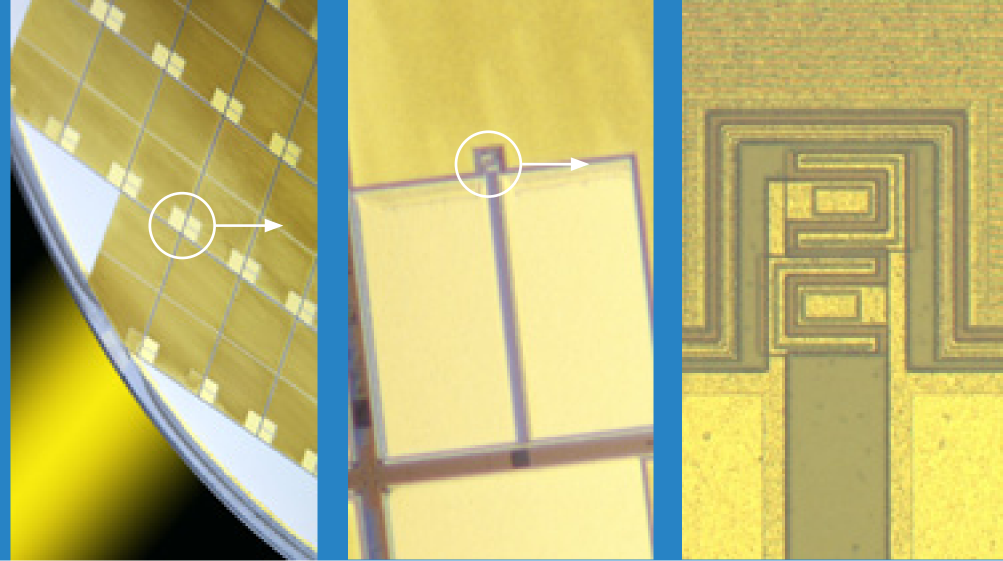


Figure 2: PowerMOS device with implemented diode for temperature measurement

POWERMOS DEVICES CUSTOM-DESIGNED FOR THE CENTER OF COMPETENCE FOR POWER ELECTRONICS IN SCHLESWIG-HOLSTEIN

A significant part of the primary energy consumption is used for the generation, conversion, distribution and utilisation of electrical energy. Power Electronics has the potential to save energy along the whole supply chain from its generation up to the end user. For instance, the dominating proportion of this electrical energy is applied for motor drive applications. Here, the intelligent use of Power Electronics is estimated to save electrical energy up to 20–30 %.

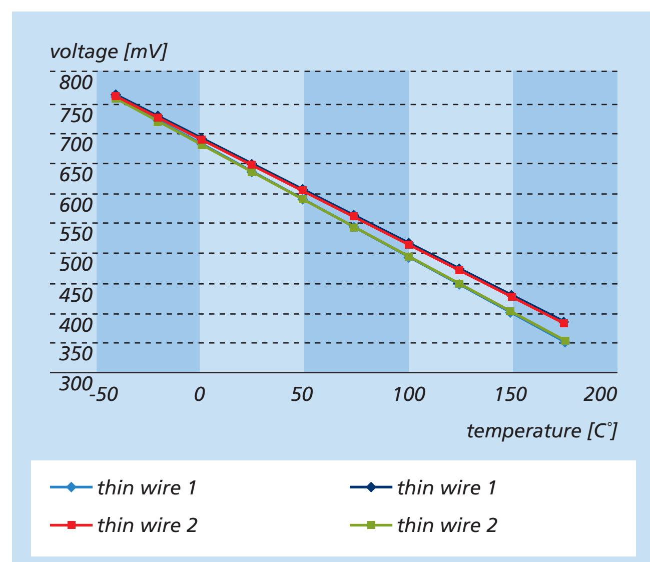
Power Electronics is a cross-sectional task. Beginning with semiconductor power devices and ending at complete power systems, many technological and economical challenges have to be considered and to be solved. Beside the costs reliability, lifetime, power density and efficiency are the main topics to characterise the performance of electronic components and systems.

Within the Center of Competence for Power Electronics, a start up project was initiated with the objective to develop a power converter for industrial application which is optimized with respect to the topics mentioned above. For this purpose a complementary team of industries, universities and institutes located in Schleswig-Holstein was established covering the entire value added chain from semiconductor devices up to power electronic systems. Special project topics are the development of application specific PowerMOS devices, Power Modules, Driving Circuits and Control Electronics.

As a concrete example a power module is being optimized with respect to lifetime, reliability, advanced assembly techniques and optimized DCB layout for minimum parasitic inductances. The leadframe with DCB assembled with the new PowerMOS devices is shown in figure 1. Here, the backside of the chips are mounted by Ag sintering technique (Fachhochschule Kiel) whereas the frontside was wire bonded in first tests.

The development of the PowerMOS device was carried out in collaboration with Vishay based on a qualified production technology. The chip was designed for a nominal

Figure 3: Calibration curve of the temperature sensor diode



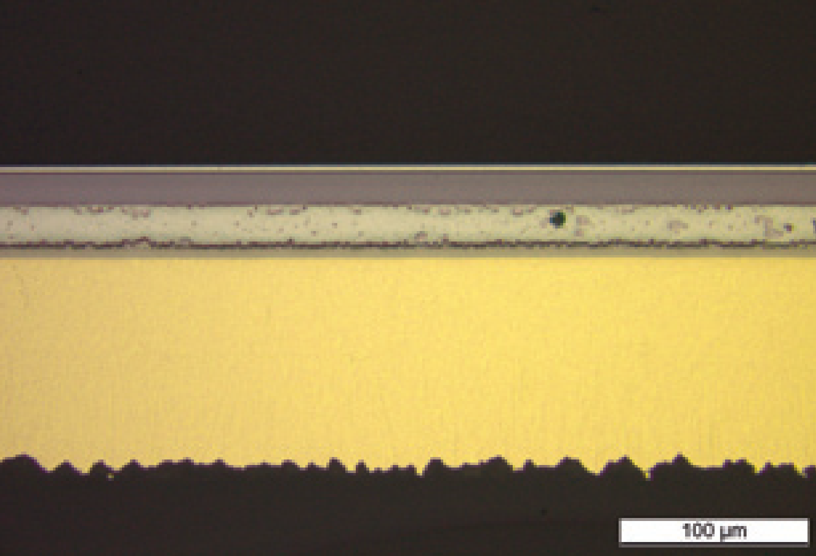
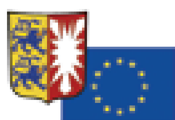


Figure 4: PowerMOS thinned down to 20 µm and soldered on a PCB

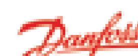
current of 150 A with a breakdown voltage of 60 V. The On-Resistance RDSon was measured in the range of 0,8 mOhm which was predicted by device simulations. The chip geometry and the pad configuration were defined according to specifications of the optimized power module.

To enable advanced assembly techniques a Ni/Au front side metallisation was applied feasible for soldering and sintering techniques. As a special feature of the PowerMOS device a temperature sensor was integrated. A picture of the special PowerMOS devices are depicted in figure 2. The temperature characteristic of the integrated sensor is shown in figure 3 which exhibit excellent linearity with a slope of 1,9 mV/°C.

A further reduction of the RDSon by 10-15 % can be reached by extremely thinning of the PowerMOS-device down to 20 µm. Currently the wafer thickness is adjusted to 70 µm. For first assembly tests PowerMOS substrates have been grinded down to 20 µm. As depicted in figure 4, the PowerMOS chip was soldered on a thick Cu layer of a printed circuit board (PCB).



ZUKUNFTSprogramm Wirtschaft *Investition in Ihre Zukunft*

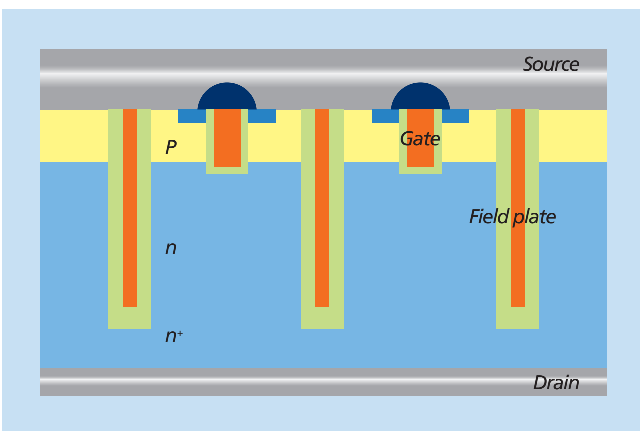


SUPER POWERMOS: COMPENSATION STRUCTURES FOR HIGH VOLTAGE APPLICATIONS

The main static parameters for a Power-MOSFET are the On-Resistance R_{DSon} and the Breakdown Voltage V_{BR}. One goal in Power-MOSFET development is to minimize the R_{DSon} under the condition of constant Breakdown Voltage which means to optimize the trade-off between these two parameters for best device efficiency.

A highly effective approach for optimization high voltage Power-MOSFETs up to 300 V is the implementation of the charge compensation principle by so called field plate structures as illustrated in figure 1.

Figure 1: Schematic cross section of a dual Gate compensation Power-MOSFET



Under blocking condition the entire drift zone region between the vertically isolated field plates and the upper p-n junction will be fully depleted. The field plates are acting as equipotential electrodes clearing up the entire drift zone from electrons and compensating the remaining space charges. Special doping profiles are required to ensure a complete depletion over the entire drift zone region in between the compensation trenches. The distance of the deep trenches (mesa width) has to be correlated with the doping concentration in order to allow a perfect charge compensation for the nominal breakdown voltage.

Due to this compensation principle it is possible to use higher doping concentrations for the drift zone region compared to standard PowerMOS devices. This helps to significantly reduce the On-Resistance under forward condition while keeping the Breakdown Voltage constant. Based on the new device concept the R_{DSon} value can be reduced by a factor of 3 for e.g. 250 V transistors.

Fraunhofer ISIT has developed first high voltage PowerMOS transistors with the new trench field plate concept on 8-inch Silicon substrates. The transistor architecture is based on deep Si trenches with an isolated Poly-Si field plate. According to the dual trench approach the compensating trenches are separated from the PowerMOS trenches as depicted in figure 2a. The PowerMOS transistor cell is located in between the deep field plate trenches as clearly seen in the SEM cross section. Within the deep trench the Poly-Si field plate is electrically isolated by a thick SiO_2 layer to the Si mesa area. However, at the upper interface the field

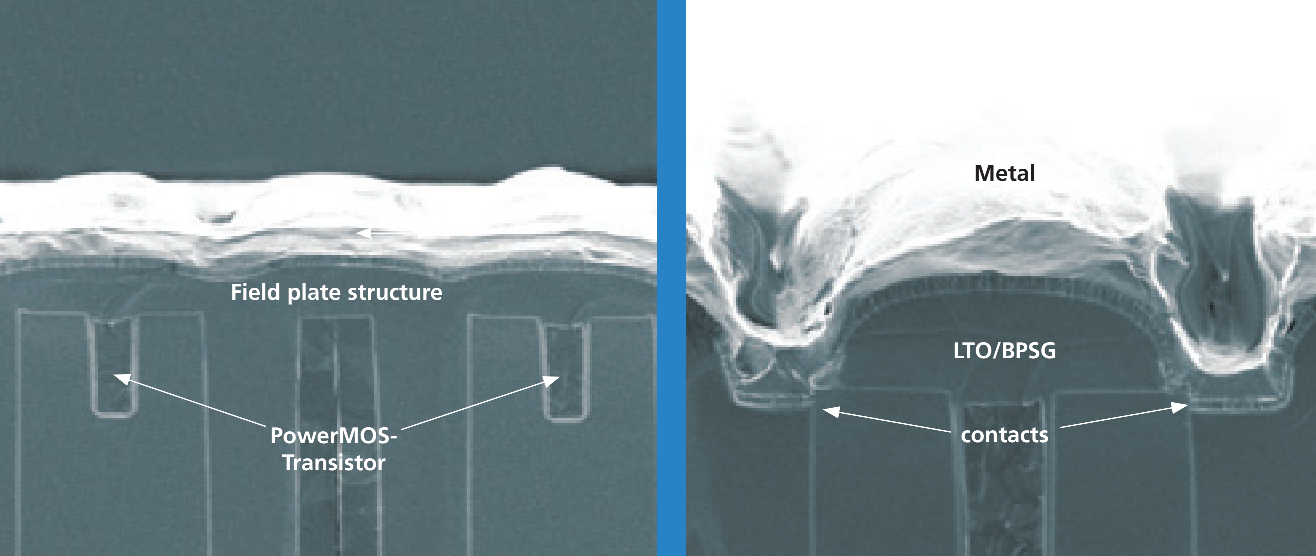


Figure 2: SEM cross section of a fully processed dual Gate compensation Power-MOSFET
a) Transistor cell with compensation structure *b) Transistor cell with Source contacts*

Figure 3: Drain characteristics of a field plate PowerMOS device for different Gate-Source voltages

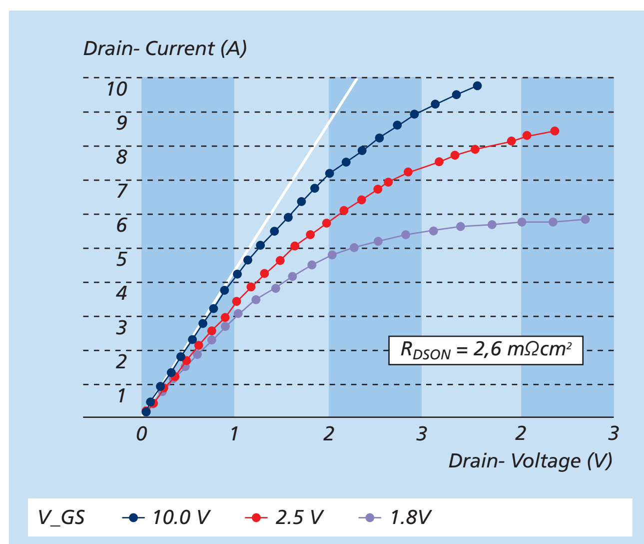


plate is connected to the Si mesa by common Source contacts. This contact scheme is depicted in the SEM cross section of figure 2b showing the overlapping contact to the mesa edge.

First electrical results have been achieved for dual trench field plate PowerMOS devices with breakdown voltages in the 200 V range. A typical I-V output characteristic is shown in figure 3 for different Gate-Source voltages. Best specific R_{DSon} values of 2.6 mOhmcm² have been measured for a Gate-Source voltage of 10 V which is good correlated to simulation results.

By integrating the compensation and the PowerMOS trench within the same trench structure further reduction of the R_{DSon} can be achieved in a so called Split-Gate approach.

Figure 4: 200 mm wafer with compensation PowerMOS devices

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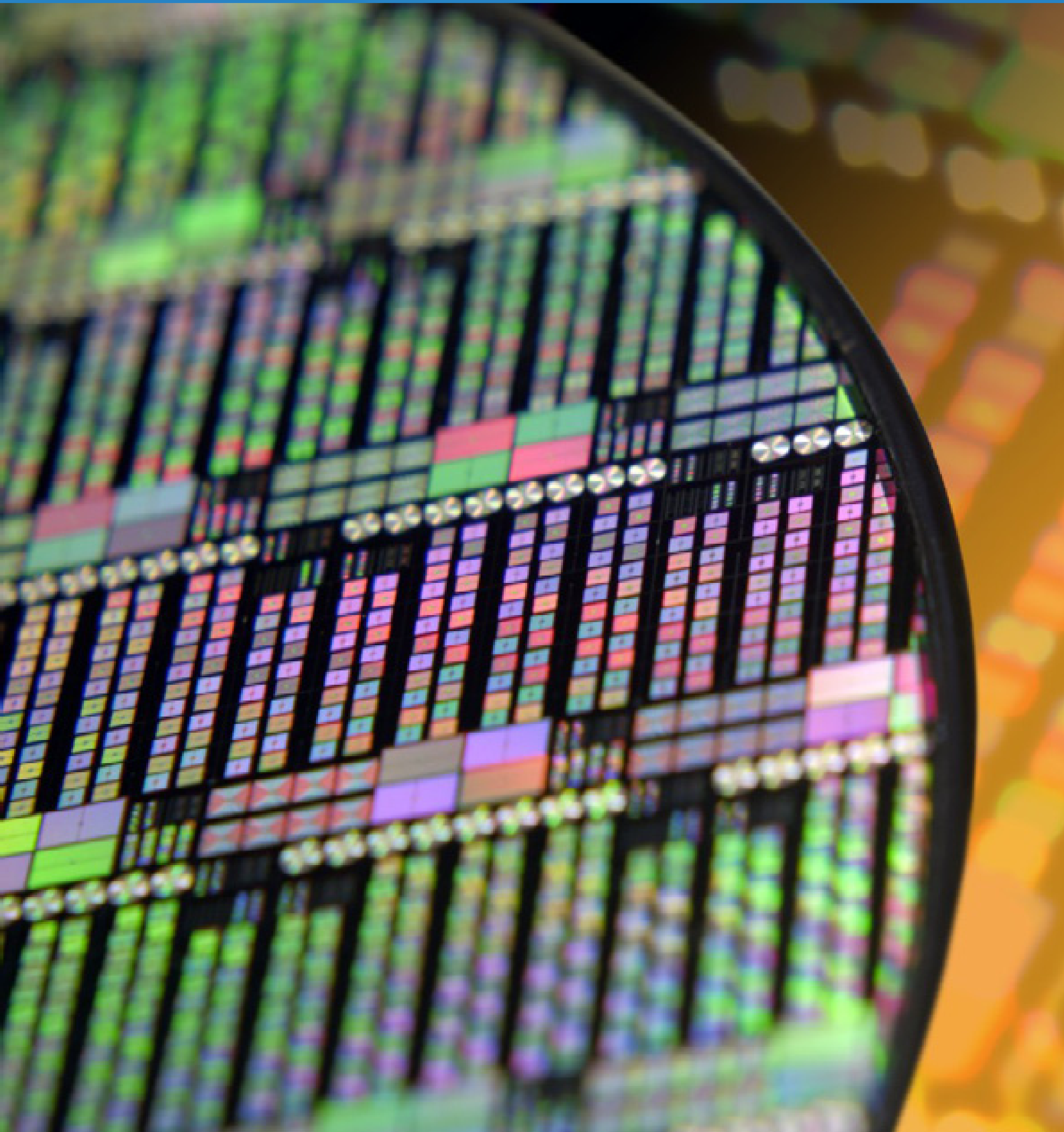


BIOTECHNICAL MICROSYSTEMS

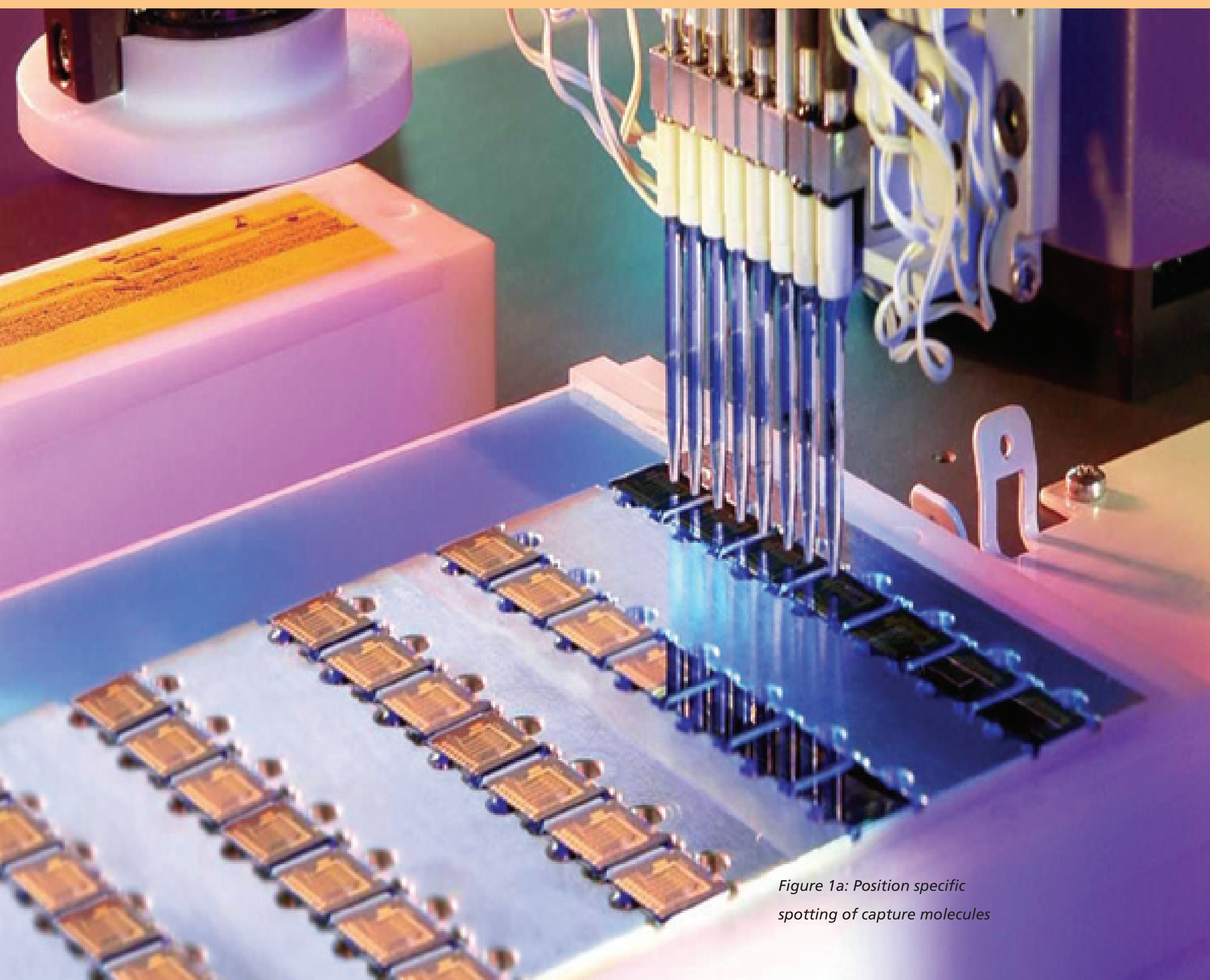


Figure 1a: Position specific spotting of capture molecules

Figure 1b: Fully automated electrical biochip system
(Chip adapter from AJeBiochip GmbH)

POINT-OF-CARE-DIAGNOSTIC-PLATFORM FOR HCV-DETERMINATION

The in vitro diagnostics occupies an increasingly central role in medical care. In particular, the findings of molecular medicine and genomics in the past few years contribute to this. At the same time there is a trend besides the central diagnostic laboratories to get closer to the patient and perform an analysis of even complex parameters in the field. This saves time and is cheaper in many cases. Especially microfluidic detection systems that provide miniaturization and automation and the possibility of multi-parameter analysis are here market-relevant. Commercially available standardized tests such as enzyme linked immunosorbent assays (ELISAs) in microtiter plates, however, are often time consuming and usually only feasible centrally in the laboratory because of their complex handling.

The department Biotechnical Microsystems (BTMS) developed a test system for rapid, decentralized and cost-effective detection of blood parameters based on electrical biochip technology. The performance of the system is shown by the detection of antibodies against hepatitis C virus (HCV) in diluted serum and whole blood samples. The qualitative and quantitative detection of these antibodies is done by an ELISA directly on a gold electrode array. A common microtiter plate immunoassay served as a reference system. BTMS worked here closely together with the Fraunhofer IME (Aachen), RWTH Aachen (Aachen), PharmedArtis (Aachen) and the University Hospital of Aachen. The array chips were produced in silicon technology on a 6 inch wafer level. They are equipped with 500 µm gold working electrodes and on chip reference and counter electrodes.

For preparing the array chips a recombinant expressed HCV Core antigen is applied on several gold electrodes using piezoelectric micro dispensing. Other electrodes are used as internal positive and negative control by spotting them with target proteins or bovine serum albumin (figure 1a). The immobilization of capture molecules is carried out by thiol-gold interaction and hydrophobic adsorption. The assay was performed completely automated by the biochip system (figure 1b).

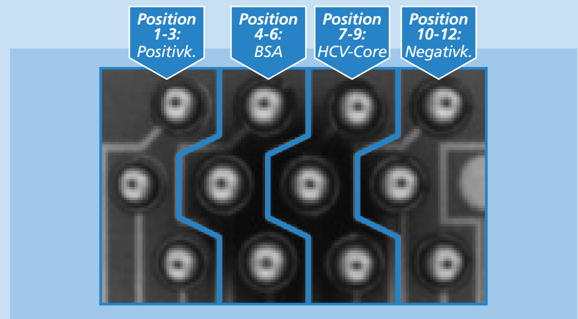
The diluted serum or whole blood samples are pumped by the internal fluidic system to the chip, where the serum antibodies to HCV bind to the HCV core antigen carrying electrodes. A subsequent enzyme labelling of these bound antibodies and the generation of an electrochemically active substrate allows the parallel and position-specific readout of the chips using "Single Electrode Redox Cycling".

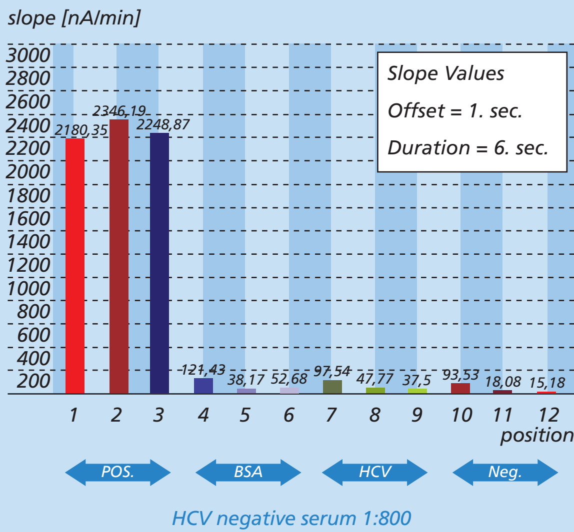
"Single Electrode Redox Cycling" uses the current enhancing effect of multiple oxidation and reduction cycles of the electrochemical active molecule 4-hydroxyaniline on a gold electrode with alternating potentials. Automatically summation of the current amounts and calculation of position specific current slopes leads to qualitative (position number) and quantitative (slope height) assay results (figure 2a).

Figure 2b shows 8 sera measured with the biochip system. Corresponding to previous tests done with a common microtiter plate ELISA 3 sera could be determined as strong HCV-Antibody positive, 2 as medium HCV-Antibody positive and 3 as HCV-Antibody negative at a dilution of 1:1600 during 20 minutes of assay time. In contrast to the microtiter plate ELISA the biochip system saved a 9-fold of assay time and a 10-fold of total reagent volume.

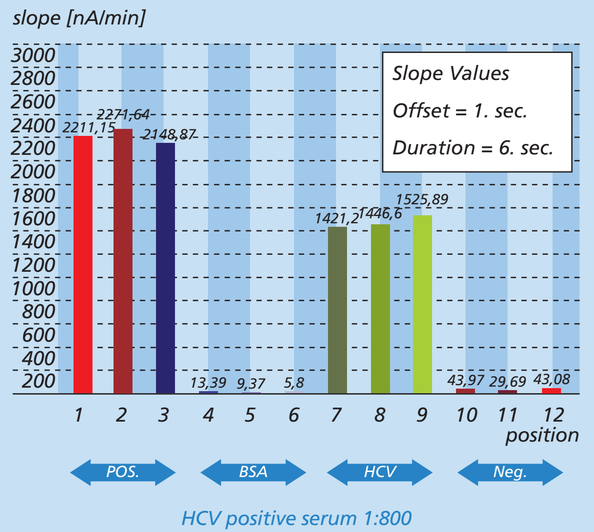
Figure 2a: Current slopes of measured serum samples

Principle:
HCV Core antigen immobilized at gold electrode arrays binds serum antibodies

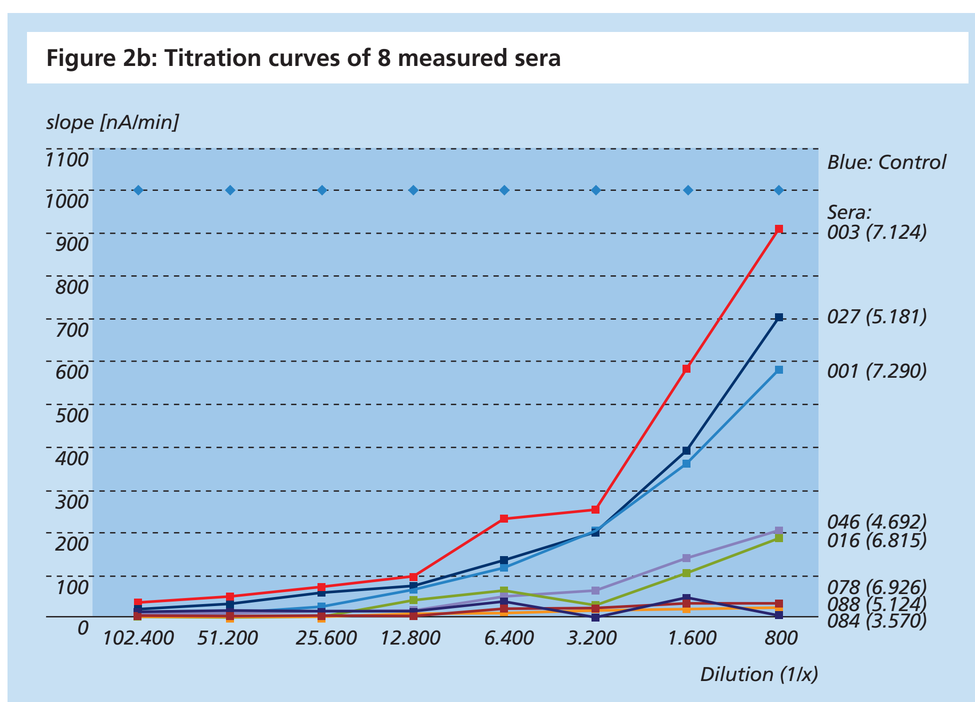




HCV negative serum 1:800



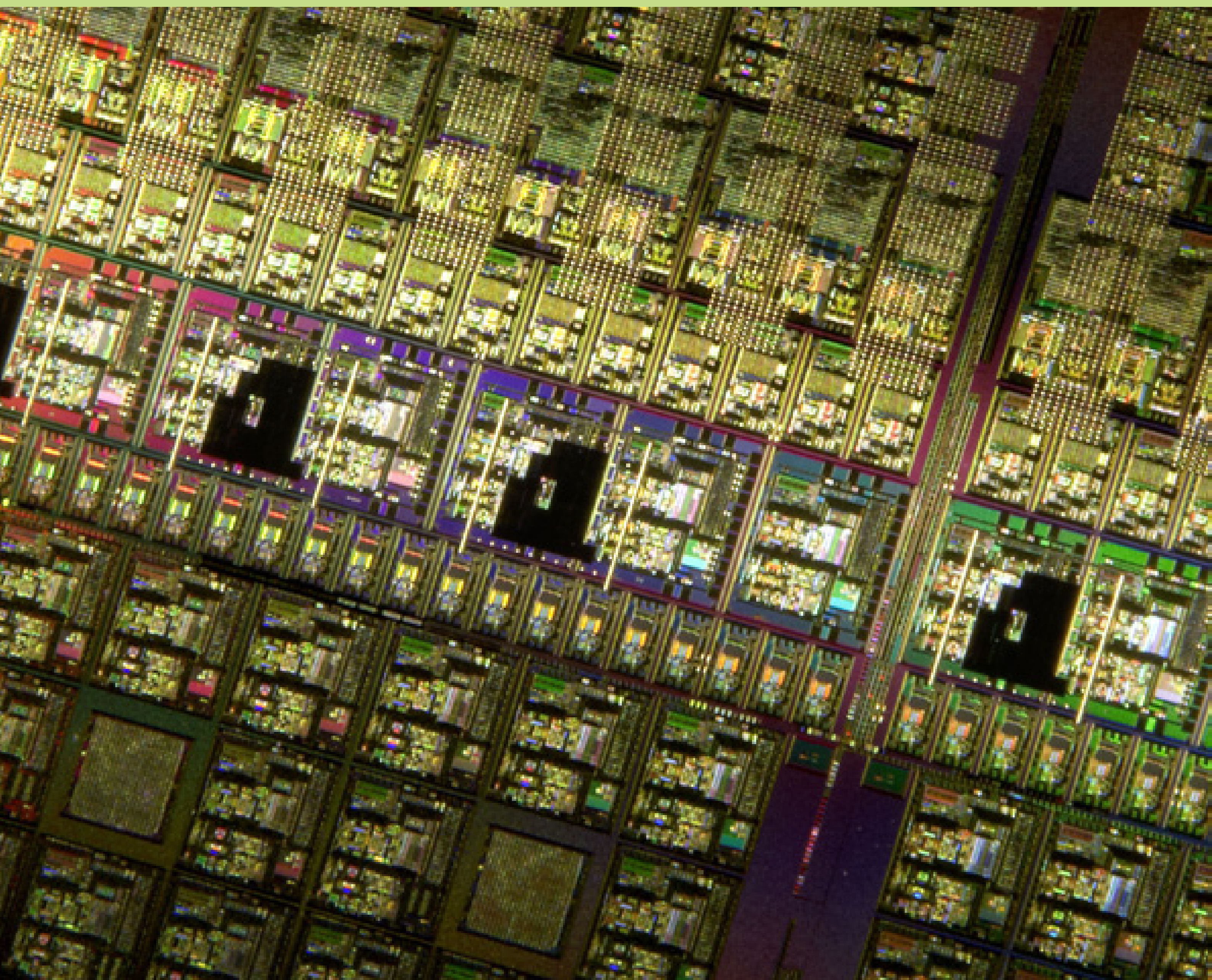
HCV positive serum 1:800



"Single Electrode Redox Cycling" is a suitable method for electrochemical detection based on an up to 40-fold current increase in relation to simple oxidation current measurements on identical electrodes. The observed current slopes are dependent on the analyte concentration (figure 2b). Multiple measurements of identical samples showed a reproducibility of +/- 7 % from chip to chip. Spiked and diluted whole blood samples could be easily measured with the same sensitivity like equivalent sera samples with no increased background signals caused by the red blood cells.

These results highlight the biochip system to be suitable for Point-of-Care applications. It is easy to handle, cost effective, fast in performing the measurements, portable and it shows high sensitivity even by measuring whole blood samples.

MODULE INTEGRATION



TESTWAFERS FOR PROCESS EVALUATION, PLACEMENT ACCURACY AND RELIABILITY TESTS

Dummy components are widely used for equipment demonstration, instruction courses, and reliability tests. The range of available components varies from small surface mount devices to all kind of chip carriers including dual-inline packages or ball grid arrays. Naked silicon dies, however, are quite rare. Fraunhofer ISIT offers as well standard designs as customized layouts for different applications:

Process evaluation and reliability tests

Flip-chip techniques are well-established alternatives to the commonly used die attach and wire bond process. Unfortunately, there is no standard process. Flip-chips can be soldered, glued with isotropic or anisotropic conductive adhesive, even combined techniques like anisotropic adhesive with solder particles (ESC5 process from Panasonic) are used. For each of these processes the reliability depends as well on process parameters as on the selected materials, e.g. flux, underfill, or glue. To establish one of these flip-chip techniques within the production of a new product several reliability tests should be performed. The left image in figure 1 shows a typical test device. Adjacent contacts are connected to realize a daisy-chain structure for lifetime tests. The device also contains a variety of fiducial marks which are used to demonstrate the alignment capabilities of pick-and-place machines.

An alternative design is shown in the right image in figure 1. This device contains two daisy chain rings with different contact pitch, i.e. 250 µm and 150 µm. In addition each daisy chain ring consists of two nested individual daisy chains. This design enables reliability tests with a voltage applied between adjacent contacts. Furthermore the resistance of each corner bump can be measured in 4point geometry.

Machine calibration and acceptability tests

Placement accuracy is a key issue of pick and place machines and wafer bonders. Fraunhofer ISIT has developed several glass wafer designs for this issue (figure 2). Each die consists of a variety of alignment marks and vernier scales, enabling automated placement, automated post bond inspection, and visual alignment analysis. Depending on the resolution of the vernier scale, placement offsets between 0.1 µm and 40 µm can be analyzed visually.

Figure 1: Testchip designs FC475 (left) and FC500 (right)

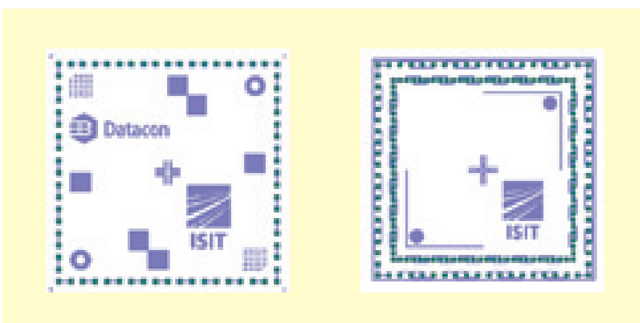
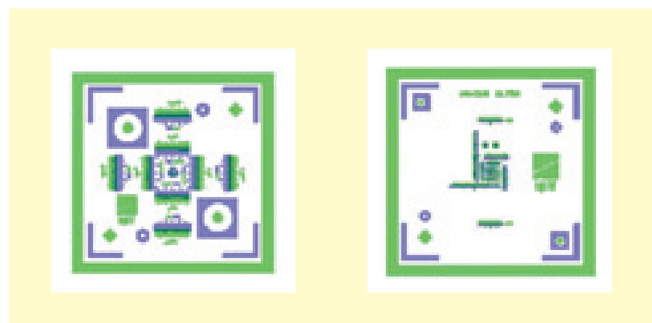


Figure 2: Glas chips „Nonius“ (left) and „Nonius Ultra“ (right). The green color corresponds to the chip wheras the blue one represents the substrate



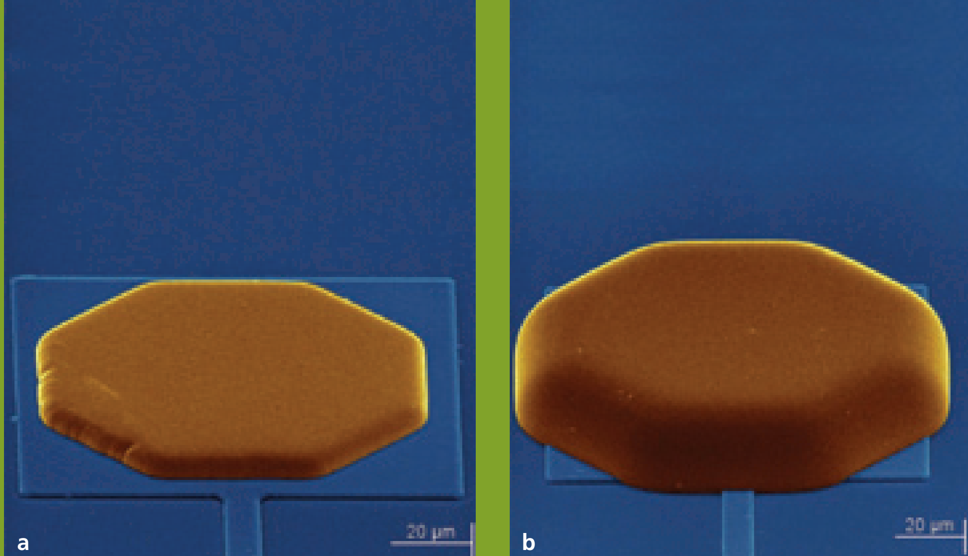


Figure 1: Colorized electron microscope images of nickel gold bumps a) 5µm high b) 20µm high

ELECTROLESS NIAU ON THINNED WAFERS ENABLES COST EFFICIENT PROTOTYPING

Electronic and PowerMOS wafers are usually fabricated in large batches and sold as single packaged die. The package sizes are permanently shrinking, nevertheless advanced products often require bare die mounting to save additional space or gain additional performance. On a large scale production level, it is quite easy to get diced or undiced wafers even with 'exotic' pad finishes. For prototyping or small scale production, however, the situation is quite different. Manufacturers usually don't like to sell single wafers – not only because of the amount of administrative work for handling and billing, but for two less obvious, but much more important reasons. First of all, wafers are usually equipped with confidential test structures that are located in the dicing street, and, second, the number of bad dies on the wafer can easily be counted – a number that manufacturers like to keep confidential.

If a prototype customer is successful in getting an undiced single wafer, what one will end up with is a standard wafer with aluminum or seldom copper bond pads. Aluminum is a perfect choice for wire bond applications, but it is useless for soldering, Ag sintering, or gluing. To overcome this material incompatibility, different pad modifications can be used as follows:

Semiconductor process based pad modifications. Utilizing the equipment of semiconductor or MEMS foundries, a variety of pad modifications including different kinds of galvanic bumps, are possible. Unfortunately, many process steps are required resulting in high initial costs for process setup and lithography masks.

Electroless NiAu (ENIG). The electroless deposition of nickel and flashgold is a pure batch process that deposits metal on any non-passivated surface. On the wafer front side, these are usually the pad openings. Since no lithography is required, the process is very cost effective for single wafer processing as well as serial production. Depending on the nickel thickness, which is usually in the range of 2 µm to 20 µm, the resulting bumps are well suited for reliable soldering, Ag sintering, or gluing applications (figure 1).

Fraunhofer ISIT offers both technologies: Semiconductor process based pad modifications, and electroless deposition of NiAu. The choice of technology depends on the final product. The semiconductor-based processes are very flexible since additional tasks like pad redistributions can be solved. However, these processes are limited to a wafer thickness of several hundred microns. If thin wafers have to be handled, an expensive rigid carrier technique has to be used. Another drawback is the required compatibility of the wafer diameter to the capabilities of the foundry. At Fraunhofer ISIT, the wafer geometry is limited to 8'' diameter.

The electroless NiAu process has less stringent requirements. The default process works on 6'' and 8'' wafers with backside passivation and standard wafer thickness. If the wafer backside is metalized, deoxidized, or subjected to backgrinding, a liquid resist or tape will be used to protect the wafer back. The tape solution is also used for thinned wafers. It has been shown that 6'' and 8'' wafers can be handled without problem at a thickness of 70 µm (figure 2). In addition Fraunhofer ISIT is also able to handle unusual, e.g. rectangular wafer geometries, or even broken wafers. (See article: Solid State Technology, April 2010, p. 20–21, Pennwell Corporation, Oklahoma)

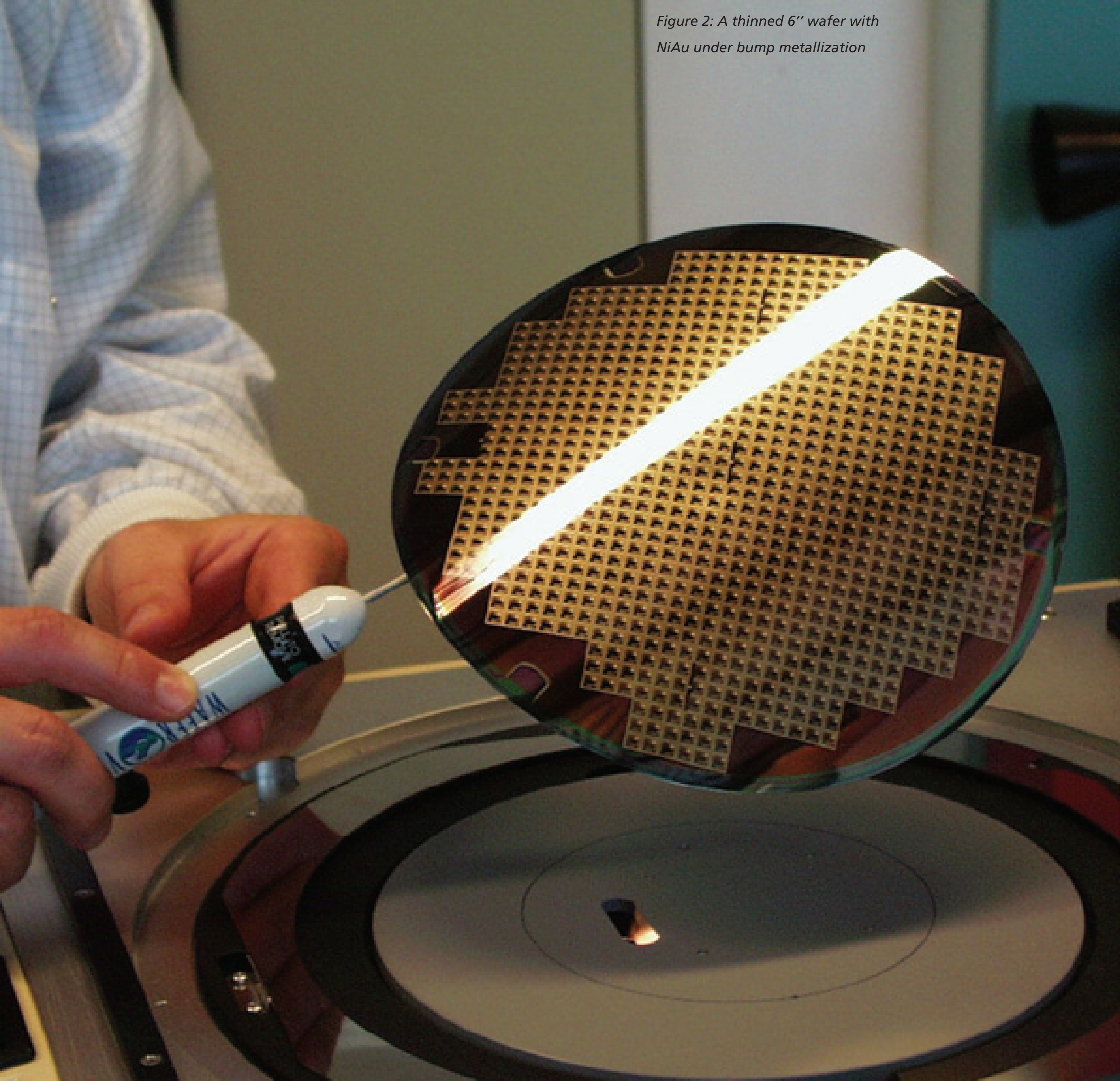


Figure 2: A thinned 6'' wafer with NiAu under bump metallization

ASSESSMENT OF THERMAL AND PROCESS PROPERTIES OF LEAD-FREE SOLDER PASTES FOR HIGH RELIABLE ELECTRONIC DEVICES

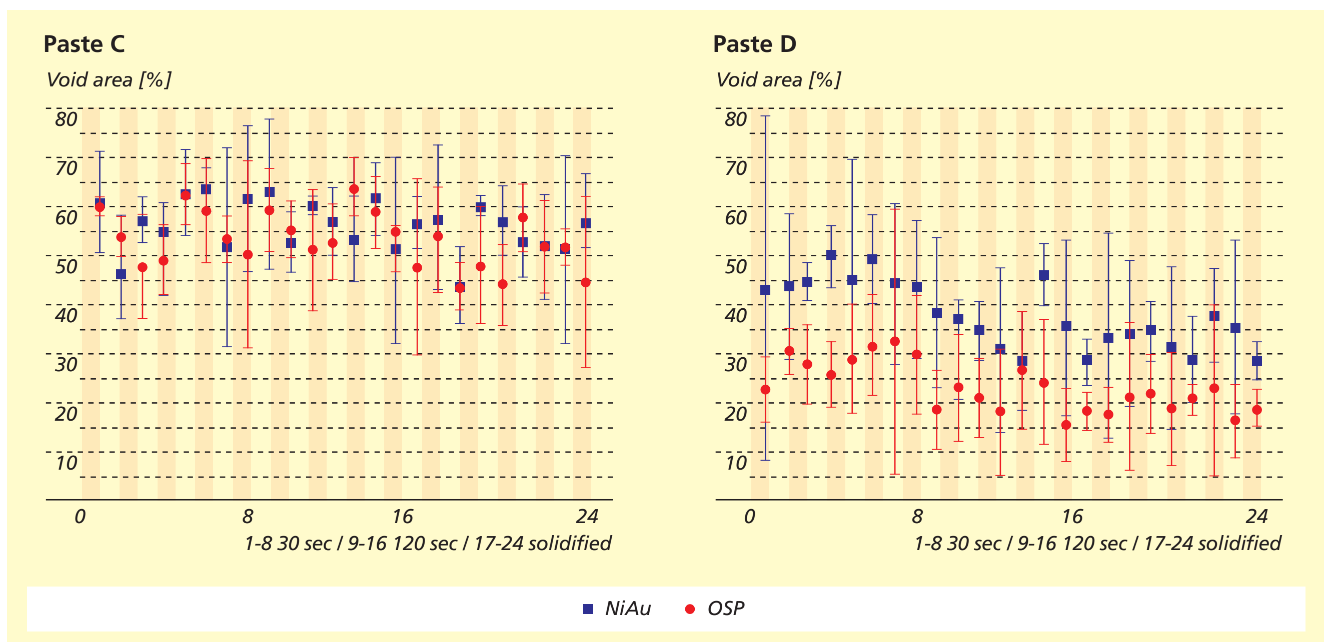
Introduction

Voids in the interior of a solder joint are not new. But during the implementation of lead-free materials void creations were observed more and more. These voids particularly lead to unwanted impairing effects in use. Voids can strongly affect the function, lifetime and shelf-life or cause increased contact resistances. Furthermore these rising contact resistances can lead to overheating of microjoints. In general the cause for all this has to be searched in the common used soldering fluxes today. The manufacturers have taken on the base flux chemistry of lead-containing pastes and used it for lead-free soldering pastes. This is one reason of the various sources which can be responsible for void creation. Flux additions have not yet solved the voiding problem. To prevent voiding expensive effortful methods like vacuum soldering or vapour phase soldering with vacuum may be used at present.

General Information

The study was part of a joint venture AiF-project (15374 N) which was conducted by the Fraunhofer IZM and Fraunhofer ISIT. For a better understanding different soldering parameters of five selected lead-free solder pastes were tested and analysed to identify parameters affecting the generation of voids.

Figure 1: Void creation paste C and paste D



In this project an X-ray compatible reflow station has been used to visualize the void generation in area soldering below 100 mm^2. The obtained data is quantified in void %-area ratio by automatic image processing during the entire reflow process. The image processing shows specific void generation profiles for each of the tested pastes with a set of process parameters. These profiles allow a deeper understanding of the paste characteristics and a more qualified selection of pastes for SMD soldering. This study includes thermal analysis performed at Fraunhofer IZM of the different pastes and fluxes additionally. Pastes and fluxes were also analyzed by using differential scanning calorimetry and thermal gravimetric analysis.

Function and Design of the Test Board

A double-sided PCB for different components was designed and applied for reflow. These boards were printed with solder paste; the components were placed, soldered and simultaneous filmed with x-ray. The PCB has different positions for four components (D-Pack, CSP, Micro-Leadframe, R0805) and eight land pattern areas (5 mm x 5 mm and 10 mm x 10 mm). The main tests and analyses were carried out for a soldering land pattern area (10 mm x 10 mm) during reflow in x-ray. In the later project phase commercial components were soldered in the reflow-oven and evaluated with x-ray. The base material of the 0.8 mm thick Eurocard (100 mm x 160 mm) consists of a FR4 epoxy resin glass fabric compound and was manufactured in accordance with IPC-735. The single board structures are milled free for the later investigations on the x-ray reflow station. The Test Board can also be transported by a typical reflow oven. This dual function makes it easier to check the used soldering profiles at the x-ray reflow station against a real soldering cycle in a reflow oven. Supplemental two different kinds of land pattern were adopted for the tests: (1) nickel / gold and (2) copper with an organic surface protection.

Solder Pastes and Test Parameters

Five different lead-free soldering pastes, which are often used for reflow soldering processes, were selected in accordance with an industrial project committee. The basic test parameters were also fixed at the beginning of the project by the involved industrial partners. The effort was limited to four influencing factors: soldering temperature, heating gradient, plateau and molten solder time. (see table 1) These selected process parameters were finally defined in a test matrix similar to a DOE matrix (Design of Experiment). It was the aim to achieve practical results. Altogether, each test was carried out three times per paste.

Void Detection and Measurement

The void creation is evaluated in the molten solder joints by X-ray transmission. With a conventional image processing program the recorded videos were taken into single pictures. These single frames were analysed after 30 seconds, 120 seconds and solidification. Later on special software was programmed and optimized from Fraunhofer ISIT so that the whole video sequences could be evaluated. The voids could also be counted and measured automatically. The ISIT software binarizes the corresponding pictures. The program counts the picture elements of the complete picture and puts them into relationship with the number of black pixels. The percentage void contents can be calculated automatically with this software tool.

Results

At the beginning all analysed data were visualized in a single diagram for each paste. The mean average values and the

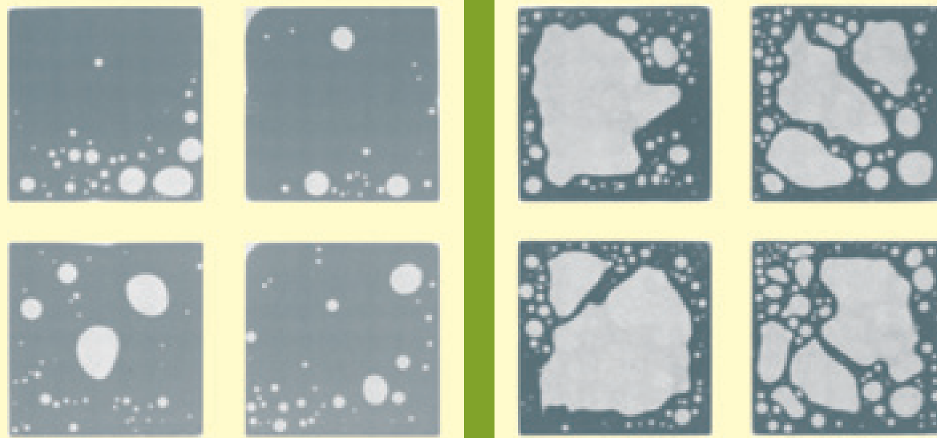


Figure 3: Sample pictures of the x-ray inspection; paste A (left) and paste C (right)

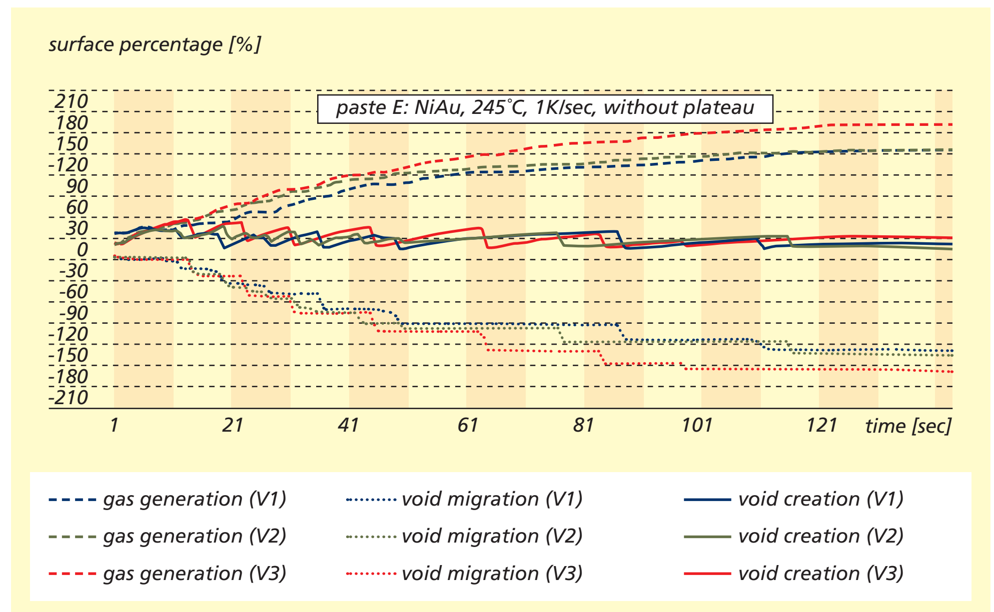


Figure 2: Dynamic behaviour of paste E

	description	factor	parameter +	parameter -
1	temperature	A	260°C	245°C
2	heating gradient	B	3 K/sec	1K/sec
3	plateau (60sec @ 180°C)	C	with	without
4	hold time	D	120 sec	30 sec

Table 1: Parameter Window

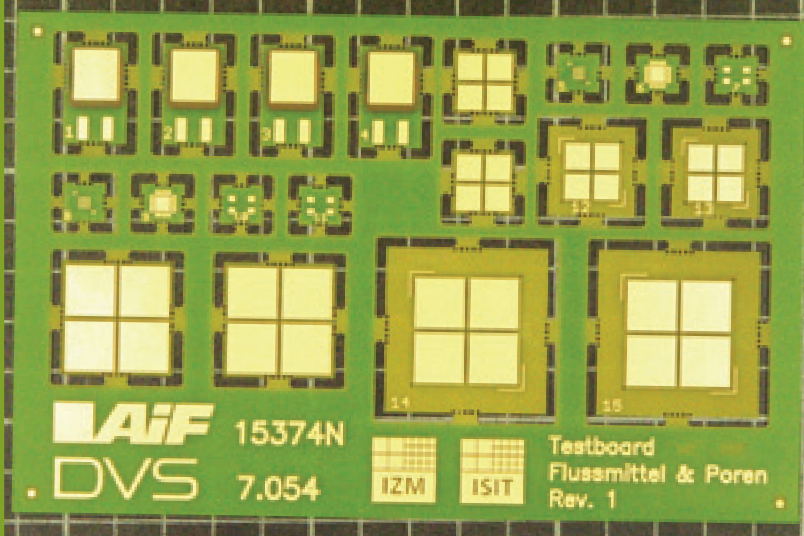


Figure 4: Test board for area soldering experiments

range are shown in figure 1 and apply to the test matrix. The void quantity in percent is shown here after 30 sec; 120 sec and after the solidification point. It was obvious that voids grew larger, with one exception of anti-tombstone paste (paste C), at all lead-free pastes in a similar manner. Paste C tends to produce more voids than the other pastes. Additional charts shows how the percent void ratio action was determined in respect to the gas generation, the void creation and the total void migration. In these charts the fluid dynamic from the molten interior of the solder joints could be shown during the reflow soldering process. The pastes showed different dynamic behaviours.

Demonstration on Demo Components

The integrated pad layouts for the different components served as demonstrators realized in the test board. For the demonstration the parameters extracted from the reflow simulation with the highest void tendency of paste C were chosen and the parameters of paste A with fewer voids were selected. This choice represents two extreme conditions, as the basis to compare reflow simulation and experimental results. This validation showed balancing behaviour.
An exception of this was monitored for CSP soldering. In this experiment the anti-tombstone paste C showed unexpectedly best results. Hardly any voids could be found.

Thermal Analysis of the Pastes

The pastes and fluxes were analyzed by using DSC and TGA. The DSC measurement was done three times for each paste at a heating rate of 20 K/min and a cooling rate of 10 K/min. The reactions of the flux are hardly visible in the DSC curve of the pastes and almost non visible in the curve of paste C. Paste C is an anti-tomb-stoning paste, i.e. it consists of two different solder spheres of different particle size. The temperature profile of the TGA of the pure fluxes was such that it was similar to a real reflow profile. In order to see what would happen if the peak temperature was hold for a longer time in a second analysis run, the peak temperature was prolonged to 30 minutes. TGA analysis reveals that the pastes / fluxes produce gas during the reflow process and that this gas production has not ceased when a normal reflow profile has ended. Even after 30 minutes the out gassing process seems to be not totally accomplished. However, there is a remarkable difference between flux A, B and D on the one hand and C and F on the other hand. While the weight of the fluxes A, B and D decreases even after 30 min, fluxes C and F reach a weight that remains constant after a few minutes already. While the main constituent of fluxes A, B and D is natural resin the fluxes C and F mainly consist of synthetic resin. TGA of the fluxes was carried in N_2 as well as in air. Unlike the pastes which due to oxidation loose more weight in N_2 than in air the pure fluxes loose more weight in air than in N_2 atmosphere.

Conclusion

This study has demonstrated that pastes tend to produce voids over the entire reflow time. The five tested pastes show different void creation and void migration with different dynamic behaviours. With the correct selection of the reflow soldering parameters the voiding can be limited under 25 % area after the solidification. Furthermore the results of the area soldering of this study can be aplied for different SMD components, with one exception of paste C at BGA components. Therefore, the development of the right reflow profile is extremely important as a contributor to the formation of voids. It is recommended to work together with the paste manufacturer to establish the reflow profile for the implementation of new solder pastes. The insitu observation of the reflow process in X-ray was found to be a very informative way to understand the melting kinetics of solder pastes.

INTEGRATED POWER SYSTEMS

LITHIUM STORAGE IN SILICON – JOINT ACTIVITY OF ISIT AND TECHNISCHE FAKULTÄT DER CHRISTIAN-ALBRECHTS-UNIVERSITÄT KIEL

Secondary Lithium ion batteries are supposed to be the most efficient means for storage of electrical power for many applications. A variety of different electrode materials are available or under development (table 1).

New emerging markets for the Lithium ion technology are the main drivers for the investigation of new electrode materials. One of the largest of such markets is electro-mobility where more and more vehicles are powered by lithium ion batteries. Here a significant improvement in the energy density is required because the state-of-the-art lithium ion batteries are still roughly 50 – to 100 – fold below that of liquid fuel. The energy density of lithium ion batteries to high degree depends on the specific capacities of the electrode materials used. For lithium cobalt oxide this is about 155 mAh/g, whereas graphite based anodes offer from 330 mAh/g to the theoretical maximum of 372 mAh/g.
Table 1 indicates that the current upper limit in the specific capacity of cathode materials may be around 200 mAh/g. On the side of anode materials, much higher specific capacities are theoretically available, compared to the standard graphitic materials. Unfortunately, these interesting materials have also major drawbacks which prohibited their use in commercial products up to now. For example metallic lithium faces critical problems with respect to safety. During charging metallic lithium can be plated on the surface of the anode and during

Table 1: Different electrode materials for rechargeable Lithium ion batteries

Cathode	Spec. cap. [mAh/g]	U vs. Li/Li+ [V]
$LiCoO_2$	155	3.5 - 4.3
$LiMn_2O_4$	140	3.7 - 4.3
$Li(Co, Ni)_yMn_{2-y}O_4$	160	4.5 - 5.0
$LiMnPO_4$	150	3.6 – 4.4
$LiFePO_4$	170	3.0 - 3.3
$LiNi_xCo_yAl_zO_2$	180	3.6 - 4.2

Anode	Spec. cap. [mAh/g]	U vs. Li/Li+ [V]
Graphite	350	0.1- 0.22
Hard carbons	> 350	0.6
Lithium	3800	0
$Li_4Ti_5O_{12}$	155	1.5
Silicon	4200	0.3
Tin	> 950	0.4 - 0.66

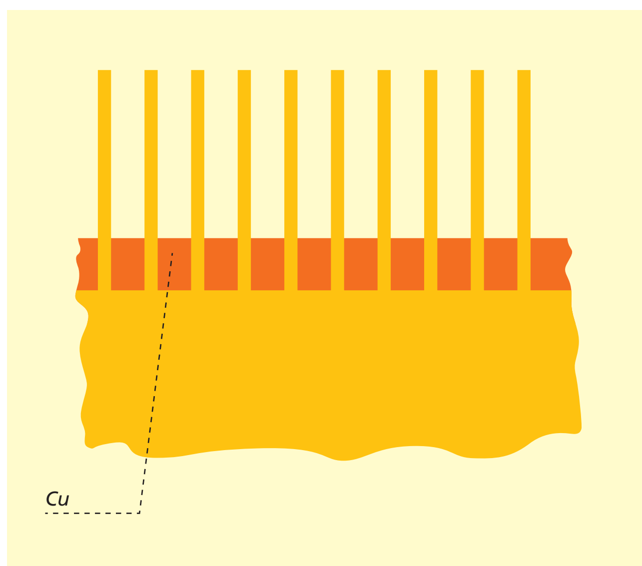


Figure 1: Schematic cross-section with Cu layer, nanowires and bulk silicon

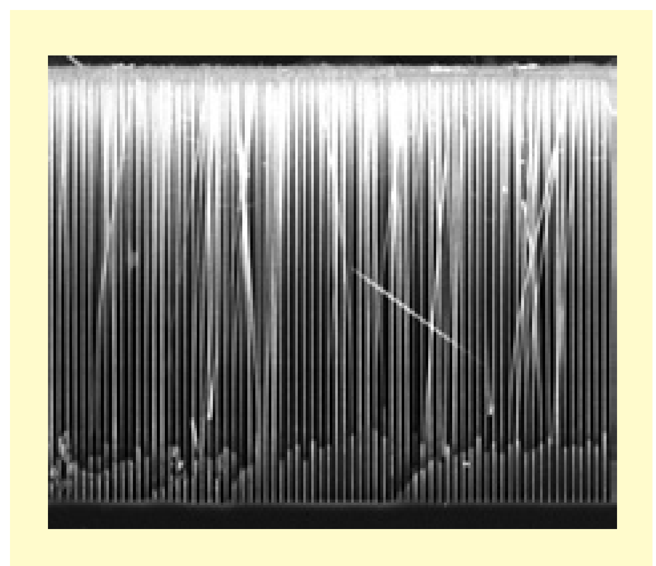


Figure 2: SEM cross-section of nanowires (diameter around 0.9 µm, lattice constant ≈ 2 µm, length 140 µm)

discharging it is redeposited on the lithium electrode. Under certain circumstances lithium may not be plated uniformly but grows as dendrites. Such dendrites can penetrate the separator and may cause internal short circuits in the cell. Tin as well as silicon have in the past already been investigated. The intercalation of high amounts of lithium in these materials during charging is accompanied by extreme volume expansion that may exceed 300%, leading to a severe amorphisation of these anode materials and mechanical fatigue upon prolonged cycling leading to a high electrode fading. Several attempts have been made to overcome these problems.
One approach is to directly grow oriented silicon nano-wires on a current collector and build complete lithium ion batteries with these anodes. Not only the theoretical specific capacity of silicon was achieved, but also a reasonable stability at low C-rate cycling was demonstrated. The underlying mechanism for why this approach leads to surprisingly good results is not yet completely understood.
The growth process of nano-wires is difficult to scale up for volume production. The group of Prof. Föll from the Technische Fakultät der Christian-Albrechts-Universität zu Kiel chose a different approach by electrochemical etching of silicon nanowires out of silicon wafers (figure 1) which is a process that has the potential for transfer into an industrial environment. Key critical issues in this kind of anode preparation is to prevent the intercalated Lithium ions from

diffusing into the bulk silicon substrate and the contacting of the nanowires with a copper based current collector (figure 1). Both problems could be solved and anodes as shown in figure 2 were obtained.

Half cells as well as complete cells with silicon electrodes have been built and tested at ISIT in a joint effort which demonstrate a surprisingly good performance. The half cell results obtained against a Lithium metal electrode in a standard electrolyte LP30 (EC/DMC, $LiPF_6$) and using a glass fiber separator showed at cycling with C/5 not only excellent cycle stability (figure 3) but in addition almost the theoretical expected value of more than 4000 mAh/g could be reached.

In a second step a silicon anode was integrated into a full cell utilizing a NCM-cathode ($LiNi_xCo_yMn_2O_2$) in combination with a glass fiber separator and an electrolyte LP30 with vinylen carbonate (VC, 1%) as stabilizing additive. This cell was cycled with C/5. The charge/discharge efficiency was again better than expected (figure 4).

These surprisingly good results with by no means optimized electrodes are very encouraging and CAU and ISIT will continue to optimize this technology especially with the potential of scalability to industrial processes.

Figure 3: Anode charge/discharge efficiency in half cell set-up as a function of cycle number at C/5. The peak at cycle 45 is an artefact caused by a failure of the temperature control.

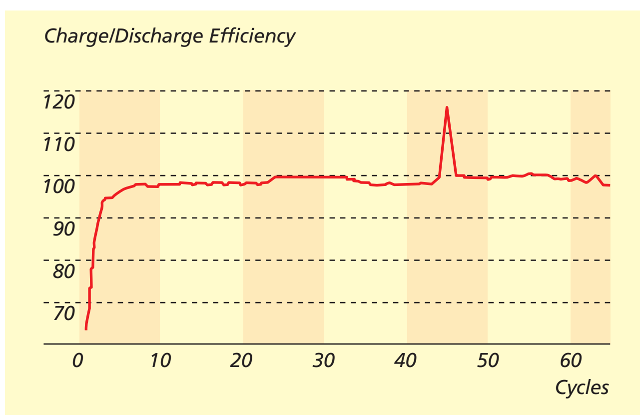
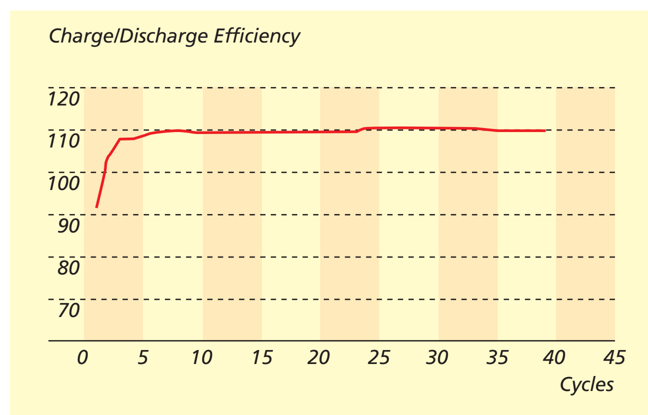
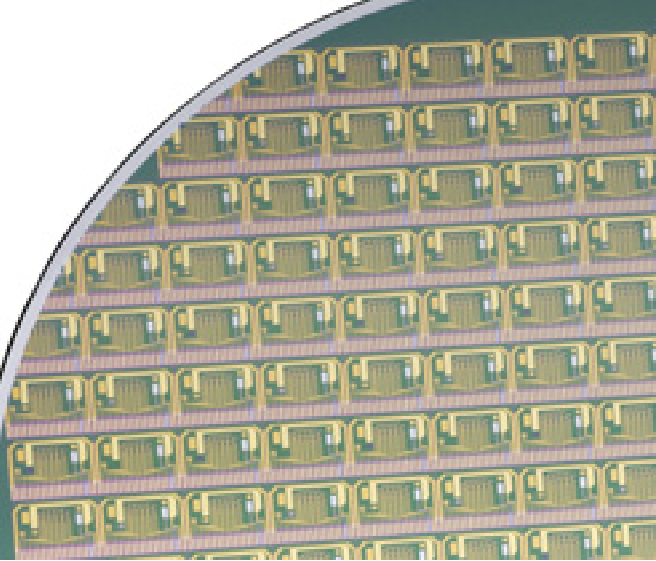


Figure 4: Full cell charge/discharge efficiency vs. cycling at C/5 of silicon anode combined with NCM-cathode in LP30 with 1% VC-additive





IMPORTANT NAMES, DATA, EVENTS

LECTURING ASSIGNMENTS AT UNIVERSITIES

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MEMBERSHIPS IN COORDINATION BOARDS AND COMMITTEES

J. Eichholz
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J. Janes
Member at MEMUNITY, The MEMS Test Community

T. Knieling
Member of GfKorr "Arbeitskreis Korrosionsschutz in der Elektronik"

R. Mörtel
Member of Forschungsgemeinschaft Erneuerbare Energien (FEE)

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Member of Netzwerk „Elektrochemie" of the Fraunhofer-Gesellschaft

G. Neumann
Member of Netzwerk „Batterien" of the Fraunhofer-Gesellschaft

G. Neumann
Member of „Verbund Energie" of the Fraunhofer-Gesellschaft

K. Pape
Member of BVS, Bonn

K. Pape
Member of FED

K. Pape
Member of VDI

M. H. Poech
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M. H. Poech
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M. H. Poech
Member of Arbeitskreis „Voids" of Frauenhofer IZM

W. Reinert
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W. Reinert
Member of Technical Committee of Electronics Packaging Technology Conference (EPTC)-Singapore

W. Reinert
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M. Reiter
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H. Schimanski
Member of ZVEI Ad-hoc Arbeitskreis Repair and Rework (R/R)

H. Schimanski
Member of DVS Fachausschuss Löten

H. Schimanski
Member of Hamburger Lötzirkel

B. Wagner
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A. Würsig
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G. Zwicker
Head of Fachgruppe Planarisierung / Fachausschuss Verfahren / Fachbereich Halbleitertechnologie und –fertigung der GMM des VDE/VDI

COOPERATION WITH INSTITUTES AND UNIVERSITIES

G. Zwicker
Member of International Executive Committee of International Conference on Planarization/ CMP Technology (ICPT)

RWTH Aachen Universität, *Aachen*

RWTH Aachen Universitätsklinik, *Aachen*

Centro National Microelectronics, *Barcelona, Spain*

Universitätsklinik Essen, Abt. für Urologie und Uro-Onkologie, Robert-Koch-Insititut (RKI), *Berlin*

Slovac Academy of Sciences, *Bratislava, Slovakia*

Intl. Centre of Biodynamics, *Bukarest, Rumania*

Cambridge University, *UK*

University of Cardiff, *Great Britain*

University of Coimbra, *Coimbra, Portugal*

Tyndall National Institute, *Cork, Ireland*

Technische Universität Dresden, Institut für Aufbau- und Verbindungstechnik

Technische Universität, *Eindhoven, Netherlands*

VTT, Espoo, Finland

University of Exeter, *Great Britain*

Fachhochschule Flensburg

LETI, CEA (Commisariat à L'Energie Atomique), *Grenoble, France*

Hochschule für Angewandte Wissenschaften, *Hamburg*

Technion, *Haifa, Israel*

Fachhochschule Westküste, *Heide*

Technische Universität, *Ilmenau*

Christian-Albrechts-Universität, Technische Fakultät, *Kiel*

Fachhochschule Kiel

École Polytechnique Fédérale de Lausanne, *Switzerland*

IMEC, *Leuven, Belgium*

Lund University of Technology, *Lund, Sweden*

IEMN, *Lille, France*

Monash University, *Melbourne, Australia*

DLR, *München*

Westfälische Wilhelms-Universität, *Münster*

CSEM, *Neuchâtel, Switzerland*

Sintef ICT, *Oslo, Norway*

Universität Oulu, *Finland*

École Polytechnique, *Paris, France*

University of Perugia, *Italy*

Drexel-University, *Philadelphia, USA*

University of Pisa, *Italy*

Süddänische Universität, *Sonderburg, Denmark*

IMS Chips, *Stuttgart*

VTT, Technical Research Center of Finland, *Tampere, Finland*

FBK, *Trento, Italy*

Fachhochschule Vorarlberg, *Austria*

Fachhochschule Wedel

DISTINCTIONS

Frank Windbracke
„Industriepreis für die herausragende Diplomarbeit im Studiengang Elektro-technik." (Charakterisierung der Herstellungstechnologie von feldplattenbasierten Kompensationsdioden in MOS-Leistungstransistoren), FH-Westküste, February, 2009

TRADE FAIRS AND EXHIBITIONS

Hannovermesse 2009
Micro Technology trade fair, April 20 – April 24, 2009, Hannover

SMT 2009
Hybrid Packaging System Integration in Micro Elect-ronics, May 5 – May 7, 2009, Nürnberg

PCIM 2009
*International Exhibition & Conference, Power Conversion Intelligent Motion,
May 12 – May 14, 2009 Nürnberg*

Sensor 2009
The Measurement Fair, May 26 – May 28, 2009 Nürnberg

Laser 2009
Trade fair for optical tech-nologies, June 15 – June 18, 2009, Munich

Productronica 2009
18 th International Trade Fair for Innovative Electro-nics Production, November 10 – November 13, 2009, Munich

Medica 2009
40th Anniversary of the World Biggest Trade Fair for Medicine, November 18 – November 21, 2009, Düsseldorf

MISCELLANEOUS EVENTS

Aspekte moderner Silizium-technologie
Public lectures. Monthly presentations, ISIT, Itzehoe

Lötprozess kompakt- Der bleifreie Lötprozess in der Elektronikfertigung
Seminar: February 17. – February 20., 2009, ISIT, Itzehoe

SMT-Rework-Praktikum
Auch mit bleifreien Loten Seminar: April 22 – April 24, 2009, ISIT Itzehoe

22. CMP Users Meeting, *April 24, 2009, BASF SE, Ludwigshafen*

Pressconference „BMBF gibt Startschuss für ISIT-Erweiterung in Itzehoe“ *Speakers: Thomas Rachel, Parliamentary State Secretary of Federal Ministry of Education and Research, Prof. Ulrich Buller, Member of Executive Board of the Fraunhofer-Gesellschaft, Prof. Wolfgang Benecke, ISIT-Director, April 30, 2009, ISIT, Itzehoe*

Kompetenzzentrum Leistungselektronik Schleswig-Holstein
First public Status Seminar: June 18, 2009, ISIT, Itzehoe

ISIT presentation in the framework of „Unternehmerfahrt 2009“
organized by Ministry of Science, Economic Affairs and Transport of the State of Schleswig-Holstein May 29, 2009, ISIT, Itzehoe

Pressconference „Land unterstützt die Modernisierung des Fraunhofer ISIT“
Speakers: Peter Harry Carstensen, Minister-President of the State Schleswig-Holstein, Prof. Wolfgang Benecke, ISIT Director, Prof. Franz Faupel, Faculty of Engineering, CAU Kiel, Hubertus Christ, Chief Executive Officer of Sensordynamics, June 15, 2009, ISIT-Itzehoe

ISIT presentation in the Framework of Pressconference „Forum Elektromobilität“ *with Prof. Annette Schavan, Federal Minister of Education and Research, September 9, 2009, Berlin*

Award „Partner der Feuerwehren“ for ISIT, Sensor Dynamics and Vishay
initiated by Feuerwehrverband Kreis Steinburg, September 24, 2009, ISIT, Itzehoe

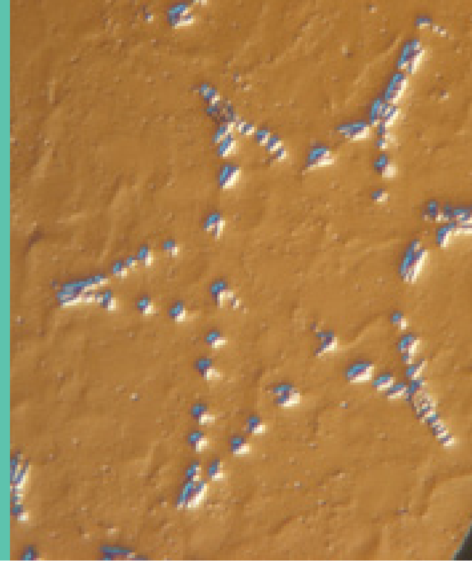
Nanomaterialien in elektrotechnischen Systemen
Seminar of Norddeutsche Initiative Nanomaterialien: September 30, 2009, ISIT, Itzehoe

23. CMP Users Meeting, *October 09, 2009, Technical University Dresden*

ISIT Presentation in framework of "Science Summer School Itzehoe",
Initiated by Hightech Itzehoe, October 26, 2009

ISIT presentation in framework of „Macht mit bei Mint – Zukunftsberufe für Frauen“, *Information day for schoolgirls, initiated by Volkshochschulen Kreis Steinburg, October 27, 2009, ISIT, Itzehoe*

Der optimierte Rework-Prozess, *Seminar. November 18 – November 20, 2009, ISIT Itzehoe*



JOURNAL PAPERS, PUBLICATIONS AND CONTRIBUTIONS TO CONFERENCES

T. Ahrens, M.-H. Poech
Beschleunigte Zuverlässigkeitsprüfung bleifreier Flachbaugruppen ist konstruktionsspezifisch – der Anwender benötigt eigene Versuche.
DVS Berichte, Band 254, DVS Media GmbH, Düsseldorf, p. 95 – 103, 2009

L. Bertels, M.-H. Poech, M. Hutter, T. Thomas
Assessment of Thermal and Process Properties of Lead-free Solder Pastes for high Reliable Electronic Devices.
Proceedings of IMAPS, Nordic Annual Conference, Tonsberg, Norway, September 13 –September 16, 2009

L. Bertels, M.-H. Poech, M. Hutter, T. Thomas
Untersuchung zu den thermischen und prozesstechnischen Eigenschaften von Flussmitteln für bleifreie Lotlegierungen auf hochzuverlässigen Baugruppen.
Deutsche IMAPS-Konferenz, Munich, October 27 – October 28, 2009

B. Elsholz, A. Nitsche, J. Achenbach, H. Ellerbrook, L. Blohm, J.Albers, G. Pauli, R. Hintsche, and R. Wörl
Electrical Low Density Microarrays for Highly Sensitive Detection of Multiplex PCR Products from Biological Agents.
Biosensors and Bioelectronics 24 , p. 1737–1743, 2009

U.Hofmann, S. Baumann, M. Oldsen, J. Janes, B. Wagner
Waferlevel-Vakuum gekapselte 2D-Mikrospiegel-Scanner für kompakte Laserprojektions-Displays im Automobil. Proceedings of Mikrosystemtechnik-Kongress Berlin, October, 2009

M. Hutter, L. Bertels, T. Thomas, M.-H. Poech
Zusammenhänge zwischen den thermischen und prozesstechnischen Eigenschaften von Flussmitteln und der Porenbildung in Lötstellen.
Schweißen und Schneiden Band 61, Heft 11, p. 644–648, 2009

M. Kandler, P. Merz, A. Foroutan, K. Reimer
Kombinierte, ausfallsichere Beschleunigungs- und Drehratensensoren für die Automobilindustrie.
Proceedings of 3. Tagung Sensoren im Automobil, München, 17. März–18. März 2009

P. Lange, S. Gruenzig, N. Marenco, W. Reinert, S. Warnat
Integration of Sensor Chips on ASIC Wafer: Selected details.
Proceedings of Smart System Integration, 2009 Brüssel

P. Lange, S. Gruenzig, N. Marenco, W. Reinert and S. Warnat
Ausgewählte Prozesstechnologien für eine Chip zu Wafer Integration von MEMS und ASIC.
Proceedings of Mikrosystemtechnik-Kongress Berlin, October, 2009

N. Marenco W. Reinert, S. Warnat, P. Lange, S. Gruenzig, G. Allegato, G. Hillmann, H. Kostner, W. Gal, S. Guadagnuolo, A. Conte, K. Malecki, K. Friedel
Investigation of Key Technologies for System-in-Package Integration of Inertial MEMS.
Proceedings of DTIP, Design, Test, Integration & Packaging of MEMS/MOEMS, April 1–April 3, 2009, Rome, Italy

P. Merz, B. Wagner, R. Dudde, W. Benecke
MEMS Foundry – Erfordernisse und Herausforderungen.
Proceedings of Mikrosystemtechnik-Kongress 2009, Berlin, p. 164–167, VDE Verlag, 2009

P. Merz, K. Reimer, M. Weiß, O. Schwarzelbach, C. Schröder, A. Giambastiani, A. Rocchi, M. Heller
Combined MEMS Inertial Sensors for IMU Applications.
Proceedings of Mikrosystemtechnik-Kongress 2009, Berlin, p. 461–463, VDE Verlag, 2009

P. Merz, W. Reinert, O. Schwarzelbach, K. Reimer
A Novel Multi Pressure Wafer Level Packaging Technology.
Proceedings of WaferBond `09, Conference on Wafer Bonding for Microsystems, 3D- and Wafer Level Integration, Grenoble/France, 2009

Mohaupt, Beckert, Bukhardt, Hornaff, Damm, Eberhardt, Tünnermann, Döring, Reimer
Precisely assembled Multi Deflection Arrays – Key Components for Multi Shaped Beam Lithography.
Proceedings of 35th Micro-NanoEngineering Conference, Ghent, Belgium,September 28–October 1, 2009

M. Oldsen, U. Hofmann, J. Janes, J. Quenzer, B. Wagner
Waferlevel Vacuum Packaged Microscanners: A High Yield Fabrication Process for Mobile Applications. Journal Integrated Circuits and Systems, 2009

K. Reimer, P. Merz, M. Weiß, O. Schwarzelbach, A. Giambastiani, A. Rocchi, M. Heller
Combined MEMS Inertial Sensors. Proceedings of Micro Mechanics Europe Conference, Toulouse, France, September 20 – September 22, 2009

M. Wagner, D. Kähler et al.
Nanostructural Analysis by Atomic Force Microscopy Followed by Light Microscopy on the Same Archival Slide. Microscopy Research and Technique, February 10, 2009

DIPLOMA THESES

Michael Jeppel
Poren und Benetzung an ausgewählten Beispielen. Technische Fakultät der Christian-Albrechts-Universität zu Kiel, July, 2009

Hauke Hartz
Herstellung und Nutzung von Silizium-Nanowires als negatives Elektrodenmaterial für Lithium-Ionen-Batterien. Technische Fakultät der Christian-Albrechts-Universität zu Kiel, 2009

Andrea Hiesener
Entwicklung, Aufbau und Test von strukturierbaren Gettern in MEMS-Gehäusen. Fachhochschule Lübeck, December, 2009

Vanessa Stenchly
CMP Slurries für die Herstellung von MOS-Leistungstransitoren. Masterthesis, Fachhochschule Westküste, Heide, March, 2009

Stefan Zander
Entwicklung eines Batteriemanagementsystems für Lithium-Akkumulatoren mit Titan-Anode für den Einsatz in einem Elektrofahrzeug. Fachhochschule Kiel, 2009

Mathias Zellmer
Aufbau eines Modells zur Herstellungskostenermittlung in der MEMS-Fertigung. Fachhochschule Wedel, February, 2009

PATENTS

B. Wenk, P. Lange, W. Riethmüller, M. Kirsten
Verfahren zur Herstellung mikromechanischer Bauelemente mit freistehenden Mikrostrukturen oder Membranen, Japan 4245660

U. Hofmann, H.-J. Quenzer, M. Oldsen
Mikrosystem und Verfahren zum Herstellen eines Mikrosystems
DE 10 2007 034 888 B3

O. Schwarzelbach
Angular rate sensor featuring mechanically decoupled oscillation modes
US 7,520,169 B2

G. Neumann, P. Birke
Pasty materials with nano-crystalline materials for electrochemical components and layers and electrochemical components produced with said materials
Canada 2 370 818

TALKS AND POSTER PRESENTATIONS

T. Ahrens
Lötqualität, Lötmetallurgie, Lötoberflächen, Flussmittel. Seminar: Lötprozess kompakt, Fraunhofer ISIT, Itzehoe, February 17, 2009

T. Ahrens
Bauelemente-Trends: RoHS-Konformität IC-, Diskrete und Passive Bauelemente. Seminar: Lötprozess kompakt, Fraunhofer ISIT, Itzehoe, February 18, 2009

T. Ahrens
Baugruppen- und Fehlerbewertung: Inspektionskriterien, Bleifreie Lötstellen. Seminar: Lötprozess kompakt, Fraunhofer ISIT, Itzehoe, February 18, 2009

T. Ahrens
Knackpunkte Bleifreies Löten: Konstruktion, Prozess und Materialauswahl. Seminar: Lötprozess kompakt, Fraunhofer ISIT, Itzehoe, February 19, 2009

D. Friedrich
Power im Norden; Kompetenzzentrum Leistungselektronik Schleswig-Holstein. Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, December 2, 2009

U. Hofmann, R. Dietzel
Mikrosystemtechnisches Laserprojektionssystem zur informatorischen Fahrerassistenz – MIKLAS. Clustermeeting Fahrerassistenzsysteme, AMAA Berlin, May, 2009

U. Hofmann, S. Baumann, M. Oldsen, J. Janes, B. Wagner
Waferlevel-Vakuum gekapselte 2D-Mikrospiegel-Scanner für kompakte Laserprojektions-Displays im Automobil. Mikrosystemtechnik Berlin, October 12 – October 14, 2009

K. Kohlmann
Ultradünne Power Devices: Performanceverbesserung durch fortschrittliche Herstellungsverfahren. Seminar: Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, February 4, 2009

K. Kohlmann, J. Burggraf, G. Mittendorfer, G. Strzalka
Approaches to thin PowerMOS Wafers to less than 20 µm. Forum „be-flexible" organized by Fraunhofer IZM, November 25, 2009, München

C. Klein, E. Platzgummer, H. Loeschner, F. Letzkus, M. Jurisch, M. Irmscher, M. Witt, W. Pilz
Programmable Aperture Plate System with Integrated CMOS Electronics for Projection Maskless Nanolithography and Nanopatterning. 53th International Conference on Electron, Ion and Photon Beam Technology and Nanofabrication, Marco Island, Florida, USA, May 26 – May 29, 2009

P. Lange
Neuer Sensor zur stationären Leckortung in Wasserverteilungsnetzen.Jahrestag, Bundesvereinigung der Firmen im Gas- und Wasserfach e.V. figwa, Arbeitskreis Rohrnetzüberprüfung, Braunschweig, January 21,2009

P. Lange, S. Gruenzig, N. Marenco, W. Reinert and S. Warnat
Integration of Sensor Chips on ASIC Wafer: Selected Details. Smart System Integration, Brussel, March 10 – March 11, 2009

P. Lange
Sensors based on Micromechanical Systems. Official Introduction of the Atomic Layer Deposition Tool, Kolloquium: MEMS and ALDT. Holst Centre / IMEC, Eindhoven, Netherlands, June 18, 2009

P. Lange, S. Gruenzig, N. Marenco, W. Reinert, S. Warnat
Ausgewählte Prozesstechnologien für eine Chip zu Wafer Integration von MEMS und ASIC. Mikrosystemtechnik Berlin, October 12 – October 14, 2009

N. Marenco, W. Reinert, S. Warnat, P. Lange, S. Gruenzig, G. Allegato, G. Hillmann, H. Kostner, W. Gal, S. Guadagnuolo, A. Conte, K. Malecki, K. Friedel
Investigation of Key Technologies for System-in-Package Integration of Inertial MEMS. DTIP, Design, Test, Integration & Packaging of MEMS/MOEMS. Rome, Italy, April 1–April 3, 2009

P. Merz
MEMS-Foundry – Erfordernisse und Herausforderungen. Mikrosystemtechnik Berlin, October 12 – October 14, 2009

G. Neumann
Lithium-Akkumulatoren für die Elektromobilität: Erwartungen, Realität, Alternativen. AktivRegion Nordfriesland Nord, Bredstedt, October 9, 2009

G. Neumann
Lithium-Akkumulatoren: Stand der Technik und Forschung. Kolloquium der Technischen Fakultät der Christian-Albrechts-Universität zu Kiel, Kiel, June 8, 2009

G. Neumann
Nanomaterialien in Lithium-Akkumulatoren. Norddeutsche Initiative Nanomaterialien NINA, Itzehoe, October 2, 2009

G. Neumann
Lithium-Akkumulatoren: eine vielseitige Technologie für unterschiedliche Anwendungen. Carl-Crantz-Gesellschaft, Pfinztal, May 7, 2009

M.-H. Poech
Das Reflow-Lötprofil unter dem Zeichen Bleifreier Ferti-

gung, Temperaturverteilung in der Baugruppe. Seminar: Lötprozess kompakt, Fraunhofer ISIT, Itzehoe, February 17, 2009

M.-H. Poech
Modellierung der thermischen Vorgänge im Reflow-Lötprozess. Seminar: Lötprozess kompakt, Fraunhofer ISIT, Itzehoe, February 2009

M.-H. Poech
Voiding – Ursachen und Wirkung. 12. Europäisches Elektroniktechnologie-Kolleg, Colonia de Sant Jordi, Mallorca, March 18 – March 22 2009

G. Piechotta
Implantate zur Vitaldiagnostik. Workshop: Implantate zur Erfassung von Vitalparametern, METEAN, Erlangen, April 21, 2009

E. Nebling
Die Fraunhofer-In-vitro-Diagnostik-Plattform eine modulare Basis für die Point of Care Diagnostik. Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, September 2, 2009

E. Nebling
Portable Array-Biochip-Plattform für Bioanalytik vor Ort, Workshop Mobile, miniaturisierte Systeme zur Vitalparametererfassung. METEAN, Erlangen, October 26, 2009

E. Platzgummer, C. Klein, P. Joechl, H. Loeschner, J. Butschke, M. Jurisch, F. Letzkus, H. Sailer, M. Irmscher, M. Witt, W. Pilz
Charged Particle Multi-Beam Lithography Evaluations for sub-16nm hp Mask Node Fabrication and Wafer Direct Write. 29th Annual SPIE/BACUS Symposium, Monterey, California, USA, September 14 – September 17, 2009

W. Reinert, P. Merz, D. Kähler
The Fraunhofer PSM X2 process for extended lifetime multi-axis inertial MEMS. SEMICON WEST 2009, San Francisco, 2009

W. Reinert
Bauteilvorbereitung für 2nd level packaging durch hermetische Sensorverkappung auf Waferebene, GMM Workshop Packaging von Mikrosystemen. Stuttgart, June 23, 2009

W. Reinert
Wafer Bekugelung für ein breites Produktspektrum durch Gavitationsförderung im Vergleich zu konkurrierenden Verfahren. Technologietag Koenen, October 13, 2009

W. Reinert
Wafer Level Technolgies: Solderable Metallizations, Power Bumping and Balling. ECPE, Paris, Sept. 30, 2009

W. Reinert, D. Kähler
Poster: Hermeticity Evaluation Techniques for Wafer Level MEMS Packages. WaferBond'09, Grenoble, December 6 – 8, 2009

W. Reinert, N. Marenco:
Future Needs in Wafer Level System Integration – Moving Towards Active Cap Wafers. WaferBond'09, Grenoble, December 6 – 8, 2009

H. Schimanski
Bleifrei Reperaturlöten: Lote und Flussmittel, Löttemperatur und Wärmebeständigkeit der Materialien. Seminar: SMT-Rework-Praktikum, Fraunhofer ISIT, Itzehoe, April 22, 2009

H. Schimanski
Komplexe SMT-Baugruppen, Nacharbeit, Handhabung. Seminar: SMT-Rework-Praktikum, Fraunhofer ISIT, Itzehoe, April 22, 2009

H. Schimanski
Baugruppen- und Fehlerbewertung, Inspektion, Röntgenverfahren, Querschliffe. Seminar: SMT-Rework-Praktikum, Fraunhofer ISIT, Itzehoe, April 22, 2009

H. Schimanski
Das Reflow-Lötprofil im Zeichen bleifreier Fertigung, BMK-Forum, Augsburg, March 25, 2009

H. Schimanski
Reparatur komplexer Baugruppen, 17. FED-Konferenz, September 24. – September 26, 2009, Magdeburg

H. Schimanski
Baugruppenschonende Reparatur unter Berücksichtigung vorhandener Reparaturstandards, 17. FED-Konferenz, September 24. – 26, 2009, Magdeburg

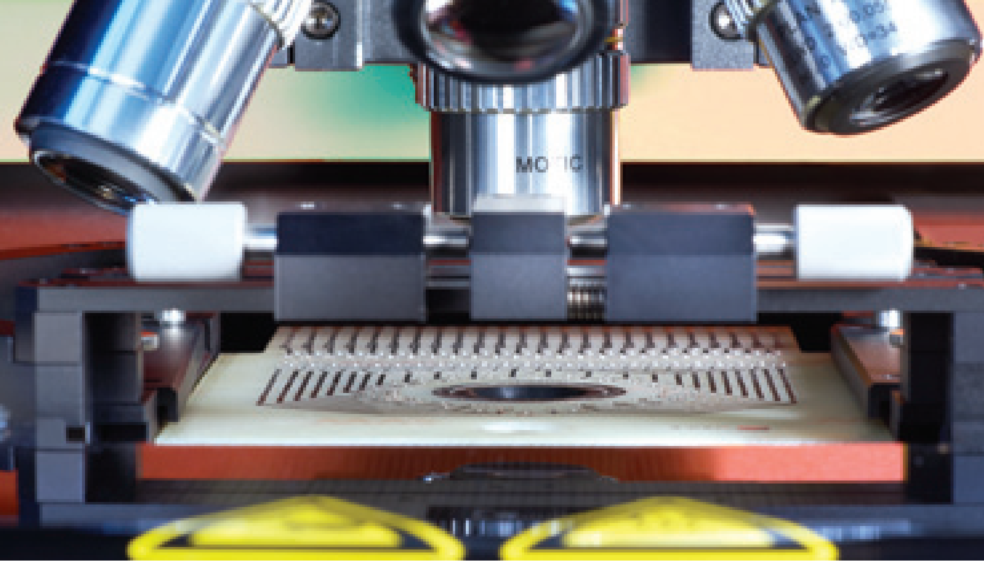
V. Stenchly
Oxid-CMP mit Ceria Slurries für SuperPowerMOS Bauelemente. Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, May 6, 2009

A. Würsig, P. Gulde, G. Neumann
Safety Aspects in Advanced Lithium Ion Batteries. ACHEMA, Frankfurt/M, May 11 – May 15, 2009

A. Würsig
Ionische Flüssigkeiten als Elektrolyte in Lithium-Akkumulatoren. Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, October 7, 2009

M. Weiss, W. Reinert, O.Schwarzelbach, K. Reimer, P. Merz
A novel multi Pressure Wafer Level Packaging Technology. WaferBond'09, Grenoble, December 6 – December 8, 2009

G. Zwicker
CMP for More Than Moore. Levitronix Conference on CMP, Santa Clara, CA, USA, February 10 – February 11, 2009



OVERVIEW OF PROJECTS

- *Development and fabrication of RF High Precision Capacitors*
- *Support for Build Up a 0,8 µm CMOS Technology*
- *Support for Build Up a 0,35 µm CMOS Technology*
- *Feedthrough and Wrap Around for Power Devices*
- *Optimierung von AMR Winkelsensoren*
- *Durchkontaktierung von Power Devices mittels W-CVD*
- *Super Junction PowerMOS*
- *Ultrathin Trench IGBTs on sub-100 µm Si-Substrates*
- *Untersuchung von Ceroxid-Dispersionen für CMP*
- *Untersuchung der Poliereigenschaften verschiedener Slurries für Cu-CMP*
- *Entwicklung von poly-Si CMP Prozessen für die MEMS Herstellung*
- *Untersuchung an mikromechanischen Drehraten-Sensoren*
- *Entwicklung von kapazitiven HF-Schaltern*
- *Durchfluss Sensoren für die Wasserwirtschaft*
- *Entwicklung von piezoelektrischen Schichten für Si-Mikroaktuatoren*
- *Ultraschallanalyse flüssiger Mehrphasengemische*
- *Herstellung mikrooptischer Linsenarrays aus Glas*
- *Mikrolinsen aus Borosilikat glas*
- *RF-MEMS Packaging*
- *Zero- and First – Level Packaging of RF MEMS*
- *MEMS Pack*
- *Drehratensensoren für Raumfahrtanwendungen*
- *Piezoelektrischer Messkopf für die Ultraschallanalytik*
- *Entwicklung von PZT-Schichten*
- *Mikroscann-Systeme für Display Anwendungen*
- *Mikrotechnische Fabrikation von Laserresonator-Spiegeln*
- *Herstellung mikrotechnischer analoger Ablenkeinheiten*
- *Charged Particle Nanotech, CHARPAN*
- *Maskless lithography for IC manufacturing, MAGIC*
- *Radical Innovation Maskless Nanolithography, RIMANA*
- *Mikrosystemtechnische Laserprojektion zur informatorischen Fahrerassistenz, MIKLAS*
- *Study on Silicon MEMS Force Sensors, SMErobot*
- *Development of an ASIC for the control of BLDC-motors*
- *Micro-Nano Integrated Platform for Transverse Ambient Intelligence Applications, MINAMI*
- *Probebased terabit memory. PROTEM*
- *Generic Manufacturing and Design Technology Platforms Based on Novel RF Technologies, RF-PLATFORM*
- *Vollautomatische Detektion biologischer Gefahrstoffe mit integrierter Probenaufbereitung, BioPROB*
- *Elektrischer DBD-ISIT-eBS-Array-Immundetektor: Beratung, Bereitstellung und Spotten von Mikrochips für den Toxinnachweis, Service*
- *Analysesystem für die markergestützte intraoperative Tumordiagnostik*
- *USDEP, Ultrasensitive Detection of Emerging Pathogens*
- *ivD-WISA, in vitro Diagnostik Plattform*
- *Chipkartenbestückung mit Grautonblenden*
- *Stressoptimierte Montage und Gehäusetechnik für mikromechanisch hergestellte Silizium-Drehratensensoren*
- *Glassfritt Vacuum Wafer Bonding*
- *Glaslotbonden mit strukturierten Capwafern und Musterwafern*
- *Automotives Mikrokamerasystem für Fahrzeugumfelderfassung, µ-CAM*
- *Downscaled Assembly of Vertically Interconnected Devices, DAVID*
- *Pan-Mobile Erfassung mit optimierten Smart-Labels zur Effizienzsteigerung von Logistikprozessen, PESEL*
- *Wafer Level Packaging*
- *Process Development for hermetic AuSn vacuum sealing of µ Bolometer Sensors on Wafer level*

- *Wafer Level Balling for 100 µm up to 500 µm Spheares*
- *Customer Specified Test Wafers*
- *Neon Ultra Fine Leak Test for Resonant Micro Sensors*
- *Solder flip chip on flex*
- *Flip chip Embedding Study and Demonstration*
- *Qualitätsbewertung an bleifreien Baugruppen*
- *Demonstration and Training Lead-Free Soldering for European Industrie, LIFE*
- *Lötwärmebeständigkeit und Zuverlässigkeit neuer Konstruktionen im manuellen Reparaturprozess bleifreier elektronischer Baugruppen (AiF-Projekt)*
- *Tin-Whisker Evaluation of Components and Assemblies with Tin Finishes*
- *Prozessoptimierung beim Selektivlöten für Anwendungen in der Leistungselektronik*
- *Assistance for Electronics Manufacturers in the Transformation to RoHS Compliant Products and Processes*
- *Untersuchung zu den thermischen und prozesstechnischen Eigenschaften von Flussmitteln für bleifreie Lötlegierungen auf hochzuverlässigen Baugruppen*
- *Entwicklung eines Mikro-Controller-gesteuerten, SOA-überwachten Halbleiter-Gleichstrom-Relais für Boardnetze*
- *ZuSi- Zuverlässiger Ag-sinterkontaktierte Halbleiterbauelemente für die regenerative Energietechnik*
- *Ionische Liquide für elektrochemische Applikationen (IL-Echem)*
- *Akkus für medizinische Anwendungen im Rahmen des EU-Projektes MINAMI (Micro-Nano integrated platform for transverse Ambient Intelligence applications)*
- *Materialscreening von Elektrodenmaterialien für Lithiumakkumulatoren zum Einsatz in Hybrid- und Elektrofahrzeugen*
- *Alterungsuntersuchungen an langzeitbetriebenen Lithiumakkumulatoren zur Solarstromspeicherung*
- *Amagnetische Lithiumzellen*
- *Flottenversuch Elektromobilität*
- *Hochenergie-Lithiumbatterien für die Zukunft- HE-LION*
- *Simulationsstudie für Fast Recovery Dioden*
- *Energie-Effiziente Elektrische Antriebstechnik: Neue Umrichterkonzepte*
- *Lochmembranen im sub-0,5µm Bereich*
- *Entwicklung neuer Ansätze für RC-IGBTs*

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HTP Architekten und Ingenieure, Braunschweig: page 9

All other pictures Fraunhofer ISIT

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