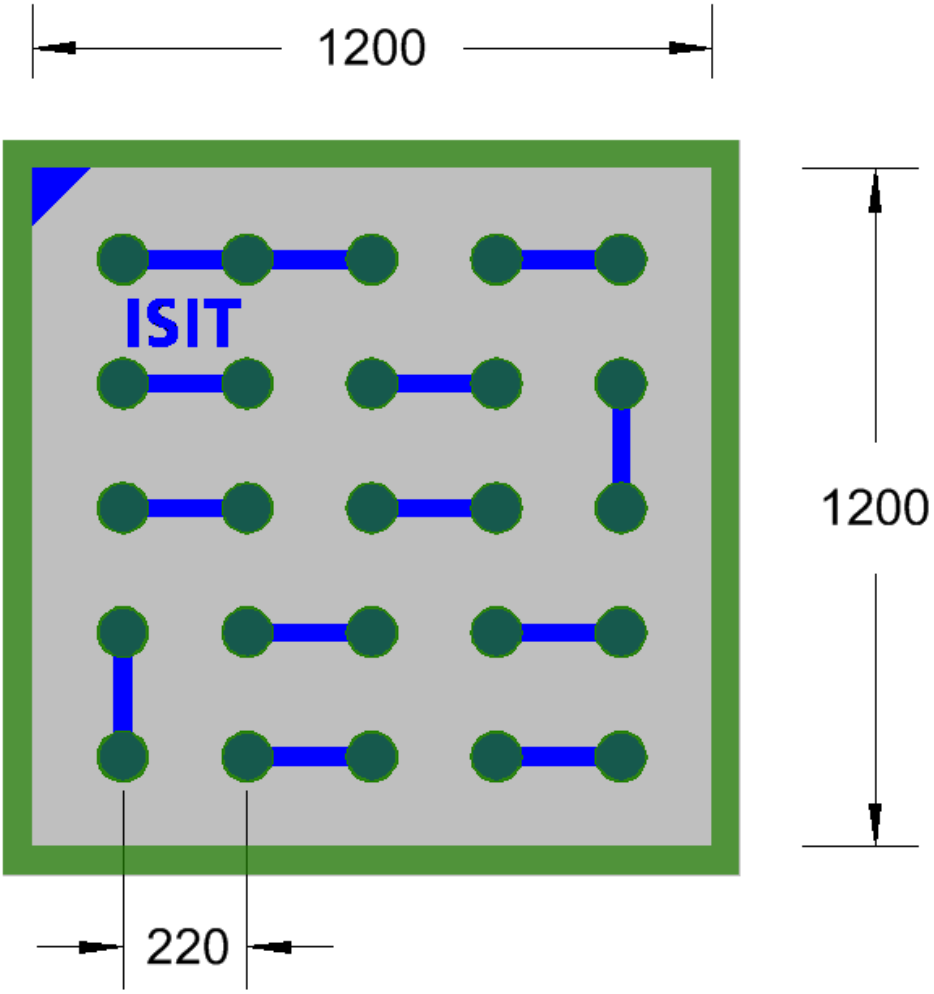
Fraunhofer ISIT	PRODUCT DATA SHEET	page: 1 of 2
	Silicon Test Wafer CSP1200-220 8''	last update 20.02.2017

LAYOUT:



TECHNICAL DATA:

- Flip Chip Silicon Die (Chip Size Package)
- dummy component with daisy chain grid contacts
- one contact designed for Kelvin probe measurement of the contact resistance
- pin one mark for automated placement
- design size 1.20 mm x 1.20 mm with 100 µm dicing street (without passivation)
- circular aluminium pads with 80 µm diameter
- circular passivation opening with 90 µm diameter
- contact pitch 220 µm
- custom specific wafer thickness
- pad modifications with electroless NiAu and 150µm solder balls or stud bumps available

TECHNICAL INFORMATION:

designed chip size	1.20 mm x 1.20 mm
die pitch	1.30 mm x 1.30 mm
typical die size after dicing	1.27 mm x 1.27 mm other geometries, e.g. 4x4 dies available on request
wafer thickness	50µm (Taiko geometry), other thicknesses available on request
pad layout	25 pads, in daisy chain geometry with 220µm pitch and 1 Kelvin sensing structures for contact resistance measurement
pad geometry	aluminum: 80µm diameter (circular) passivation opening: 90µm diameter (circular)
pad metal	1.4 µm AlCu0.5
passivation	PECVD: 300 nm LTO + 800 nm SiN
optional pad modifications	electroless NiAu with 150µm solder balls or stud bumps
delivery	8" wafer, 16768 dies, diced on tape
normal uses	High throughput die and flip chip placing from wafer feeder, automatic wire bonding, encapsulation and underfill processes, reliability tests.
typical technologies	• soldering • stud-bump bonding • anisotropic conductive adhesive flip chip (ACA / ESC5) • isotropic conductive adhesive flip chip (ICA)
available substrates	Substrates available on request
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geometry variations	Arbitrary customer-specific layouts including a company's logotype can be realised on 8" glass and silicon wafers.

* Specifications subject to change without notice.
All dimensions are approximate values, which are influenced by process variations.