



Fraunhofer

ISIT

FRAUNHOFER-INSTITUT FÜR SILIZIUMTECHNOLOGIE ISIT

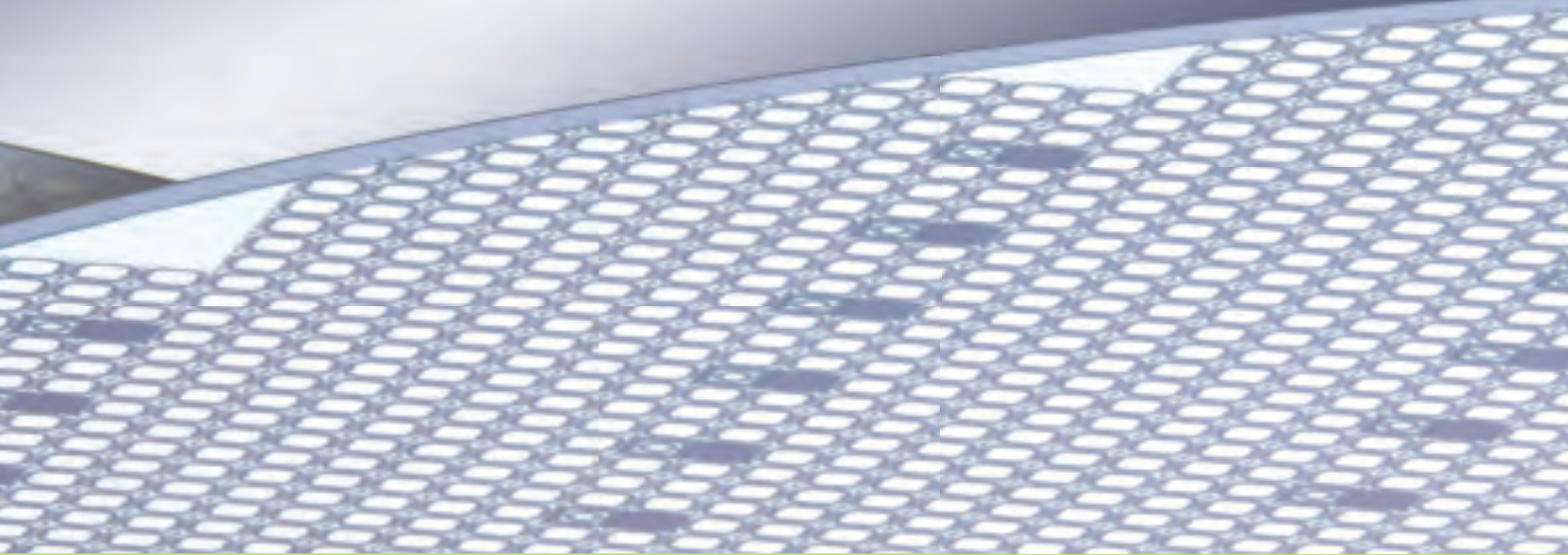
**Achievements
and Results
Annual Report**

2012



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and Results
Annual Report
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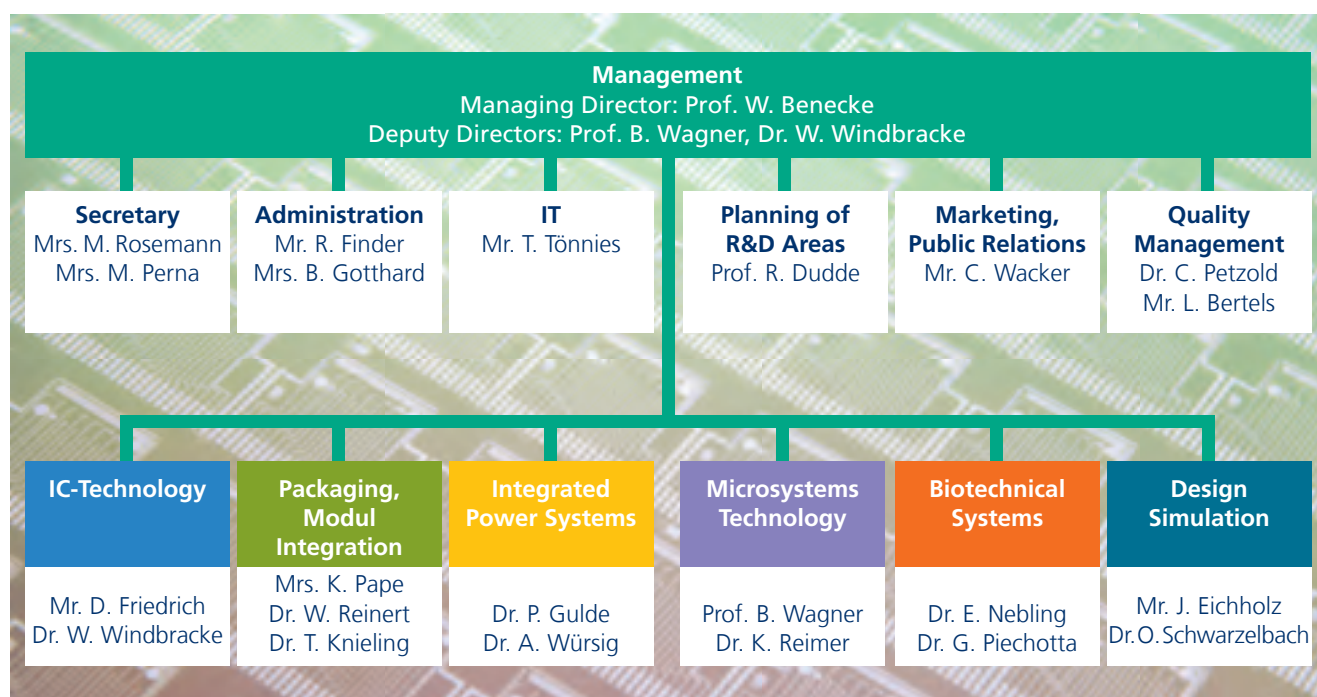
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PREFACE



ISIT cleanroom building II under construction in 2012

Organizational chart, ISIT





*Prof. Wolfgang Benecke (ISIT) and Prof. Ralf Thiericke (IZET)
discussing ISIT expansion plans*

Dear business partners, friends of the ISIT and colleagues,

I would like to take this opportunity to thank all our business partners, customers, sponsors, and friends for helping to make our collaboration so smooth and successful and for the confidence they have placed in us. It was this that allowed Fraunhofer ISIT to significantly exceed the targets for 2012.

Construction of a new cleanroom, which will serve as a state-of-the-art platform for micro-/nanosystems engineering, progressed steadily and to plan, with the topping-out ceremony held last November.

The great deal of interest shown is very much in line with the positive assessment of the location's opportunities and potential. In particular the investment in the 200 mm (8") wafer technology platform is an important strategic element in guaranteeing long-term competitiveness in the micro-/nanosystems engineering sector, both in Germany and beyond. As in previous years, the closeness of our collaboration with industrial partners at the location proved extremely intensive and innovative, and was a great help to us.

In the field of power electronics, various developments were implemented together with Vishay Siliconix in preparation for volume production of future new families of power electronics products at the location. Various strategic measures bolstered Fraunhofer ISIT's tighter focus on issues at system level. Interest and resources in the Land of Schleswig-Holstein have been pooled by setting up the Power Electronics for Renewable Energy Supply innovation cluster. The innovation cluster continues the very successful cooperation between industry, universities, and Fraunhofer ISIT, and substantially augments the portfolio. Close networking with activities in Lower Saxony, and especially with the work being done at Fraunhofer IWES,

Liebe Geschäftspartner, Freunde des ISIT und Kollegen,

allen unseren Geschäftspartnern, Kunden, Förderern und Freunden möchte ich an dieser Stelle für die gute und erfolgreiche Zusammenarbeit und das entgegengebrachte Vertrauen danken. Dies war die Voraussetzung dafür, dass das Fraunhofer ISIT auch im Jahr 2012 die Ziele deutlich übertreffen konnte.

Der Neubau eines Reinraums, als modernste Plattform für die Mikro- und Nanosystemtechnik, konnte konsequent und im Zeitplan vorangetrieben werden. Das Richtfest wurde im November des Jahres zelebriert. Das große Interesse daran hat die positive Bewertung der Chancen und Potenziale am Standort unterstrichen. Insbesondere ist die Investition in die 200mm-Wafer (8")-Technologieplattform ein wichtiges strategisches Element zur langfristigen Sicherstellung der Wettbewerbsfähigkeit im Bereich der Mikro- und Nanosystemtechnik in Deutschland und darüber hinaus. Die enge Zusammenarbeit mit unseren Industriepartnern am Standort war, so wie in den zurückliegenden Jahren, ausgesprochen intensiv und innovativ und hat uns sehr geholfen.

Auf dem Gebiet der Leistungselektronik wurden gemeinsam mit der Vishay Siliconix verschiedene Entwicklungen durchgeführt, um am Standort die Volumenfertigung neuer zukünftiger Produktfamilien in der Leistungselektronik vorzubereiten. Die verstärkte Ausrichtung des ISIT auf Fragestellungen auf der Systemebene wurde durch verschiedene strategische Maßnahmen unterstützt. Die Bündelung von Interessen und Ressourcen im Land Schleswig-Holstein ist durch die Einrichtung eines Innovationsclusters ‚Leistungselektronik für die Regenerative Energieversorgung‘ erfolgt. Das Innovationscluster setzt die sehr erfolgreiche Zusammenarbeit von Industrie, Universität, Fachhochschulen und dem Fraunhofer



*Visiting ISIT construction site: Prof. W. Benecke,
D. Austermann, H. Rickers (Mdl) and Dr. H. Helm
(from left to right)*

has proven to be a key element. In addition, talks are also underway with companies and universities in the Land of Hamburg, a region where power electronics relating to renewable energy have assumed a compelling and important position. The Fraunhofer application center model has been chosen as the model to promote in-depth cooperation, in this case with the Hamburg University of Applied Sciences (HAW). The concept was fleshed out in detail and has been submitted to those responsible pending a final decision. Meanwhile, the economic potential in Denmark, primarily in the region close to the border, is just as significant and compelling. Intensive talks for setting up a Fraunhofer research institution, as a Branch Lab of Fraunhofer ISIT, are underway with those responsible in government and in the various enterprises, with the concept being fine-tuned at present.

In microsystems engineering/MEMS, Fraunhofer ISIT is benefiting from its many years of experience in the field as well as from huge growth in interest from industry. MEMS now constitute a major integral part of electrical/electronics engineering and IT systems – and the vast array of functions supported by smartphones is just one example. A positive knock-on effect of this development is that the segment is one of Fraunhofer ISIT's fastest growing. As part of the collaboration with MAXIM Integrated Products, the transfer of the MEMS processes for inertial sensors was prepared; this paves the way for the production of high-volume applications. Fraunhofer ISIT expects to earn substantial licensing revenues from this, and stands to benefit in numerous other development and application areas from

ISIT fort und ergänzt das Spektrum wesentlich. Ganz wesentlich ist die enge Vernetzung mit den Aktivitäten in Niedersachsen, insbesondere mit den Arbeiten am Fraunhofer IWES. Ergänzend dazu wurden Gespräche mit Unternehmen und Hochschulen im Bundesland Hamburg begonnen. Leistungselektronik mit Bezug zu erneuerbaren Energien hat dort eine interessante und wichtige Position. Als Modell für eine vertiefte Kooperation wurde das Modell der Fraunhofer Anwendungszentren, hier gemeinsam mit der Hochschule für angewandte Wissenschaften HAW, ausgewählt. Das Konzept wurde im Detail ausgearbeitet und liegt den Verantwortlichen zur Entscheidung vor. Vergleichbar wichtig und interessant sind die wirtschaftlichen Potenziale in Dänemark, vorrangig im grenznahen Bereich. Mit den Verantwortlichen in der Politik und in den Unternehmen wurden intensive Gespräche zum Aufbau einer Fraunhofer Einrichtung, als Außenstelle des ISIT, geführt. Die Verfeinerung des Konzeptes findet derzeit statt.

Im Bereich Mikrosystemtechnik/MEMS profitiert das ISIT von seiner langjährigen Erfahrung auf dem Gebiet und dem massiv wachsenden Interesse der Industrie. MEMS sind heute ein fester und substanzieller Bestandteil elektrotechnischer und informationstechnischer Systeme. Die umfassende Funktionalität von Smart-Phones ist nur ein Beispiel dafür. Als positive Folge davon wächst dieser Bereich im ISIT überdurchschnittlich. Im Rahmen der Kooperation mit MAXIM Integrated Products wurde der Transfer der MEMS-Prozesse für Inertialsensoren vorbereitet, um die Fertigung für Anwendungen mit hohen Stückzahlen sicherzustellen. Das ISIT erwartet daraus erhebliche Lizenzerträge und profitiert aus dem Aufbau von Prozess- und Technologieplattformen in zahlreichen weiteren Entwicklungs- und Anwendungsbereichen. Die enge Zusammenarbeit mit der X-FAB MEMS Foundry Itzehoe wurde im zurückliegenden Jahr



Neele Lausen (right) best apprentice as 'Mikrotechnologin' at IHK Kiel and her training officer Magdalena Kontek (left)



Visitors of roofing ceremony at ISIT

setting up these process and technology platforms. The close collaboration with the X-FAB MEMS Foundry Itzehoe was steadily expanded over the past year. The offer to manufacture MEMS at the location, especially in close integration with Fraunhofer ISIT's R&D offerings, has attracted a great deal of interest from industry and has cleared the way for important, innovative new projects in the field of MEMS.

Cooperation with the University of Kiel (Christian-Albrechts-Universität, CAU) has also progressed well, with both the electrical/electronics engineering and the materials science institutes in the Faculty of Engineering. Our involvement in the SFB 855 Magnetolectric Composites research center is generating interesting impetus for new systems solutions. The efforts to create a center of competence for micro-/nanosystems engineering, affiliated to the Kiel Nanolab, were redoubled in close collaboration with Fraunhofer ISIT and applications have now been made. We expect the project to be approved in the near future.

I would once again like to thank our customers, partners in the Fraunhofer-Gesellschaft, the universities, the ministries and funding institutions at Land and federal level, project sponsors, and the EU for their trust and cooperation. My thanks go in particular to the Executive Board and central administration of the Fraunhofer-Gesellschaft, the institute coordination officer, and the members of the Advisory Board. I would also like to thank all our staff for their outstanding commitment, since without it we would not have been able to meet the targets we set ourselves.

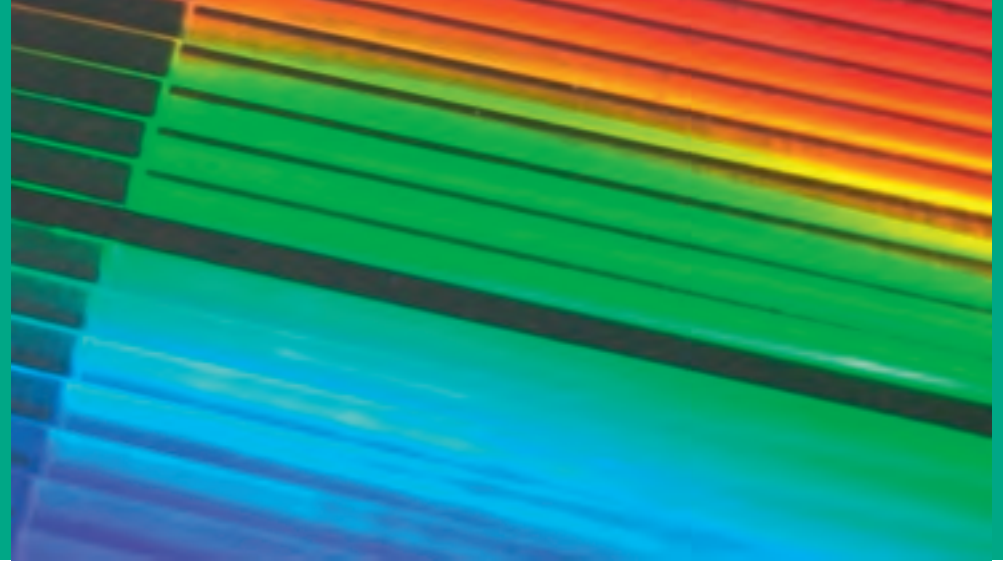
I look forward to continuing to work together with you as we strive to solve the challenges of the future.

stetig erweitert. Das Angebot zur Fertigung von MEMS am Standort, insbesondere in der engen Verzahnung mit FuE Angeboten des ISIT, stößt auf höchstes Interesse der Industrie und führte zur Anbahnung von wichtigen und innovativen Neuprojekten im Bereich MEMS.

Sehr erfreulich weitergestaltet wurde auch die Zusammenarbeit mit der Christian-Albrechts-Universität in Kiel, sowohl mit den elektrotechnischen als auch den materialwissenschaftlichen Instituten der Technischen Fakultät. Die Teilnahme am SFB 855 „Magnetoelctrische Verbundwerkstoffe“ generiert interessante Impulse für neue Systemlösungen. Die Bemühungen zur Schaffung eines Kompetenzzentrums für Mikro- und Nanosystemtechnik, angegliedert an das Kieler Nanolabor, wurden in engster Abstimmung mit dem ISIT vorangetrieben und bis zur Beantragung geführt. Eine positive Entscheidung wird zeitnah erwartet.

Ich möchte noch einmal unseren Auftraggebern, den Partnern in der Fraunhofer Gesellschaft, den Universitäten und Hochschulen, den Ministerien und Förderinstitutionen in Land und Bund, den Projektträgern und der EU für die vertrauensvolle Zusammenarbeit danken. Ganz besonders gilt dies auch für den Vorstand der FhG mit der Zentralverwaltung, dem Institutsbetreuer und den Kuratoren. Ohne das außergewöhnliche Engagement aller unserer Mitarbeiterinnen und Mitarbeiter wären jedoch die gesteckten Ziele nicht erreichbar gewesen. Dafür möchte ich mich ganz besonders bedanken.

Ich freue mich auf die weitere Zusammenarbeit und das gemeinsame Lösen zukünftiger Herausforderungen.



Test pattern of scanned laser annealing lines

FRAUNHOFER-INSTITUT FÜR SILIZIUMTECHNOLOGIE (ISIT)

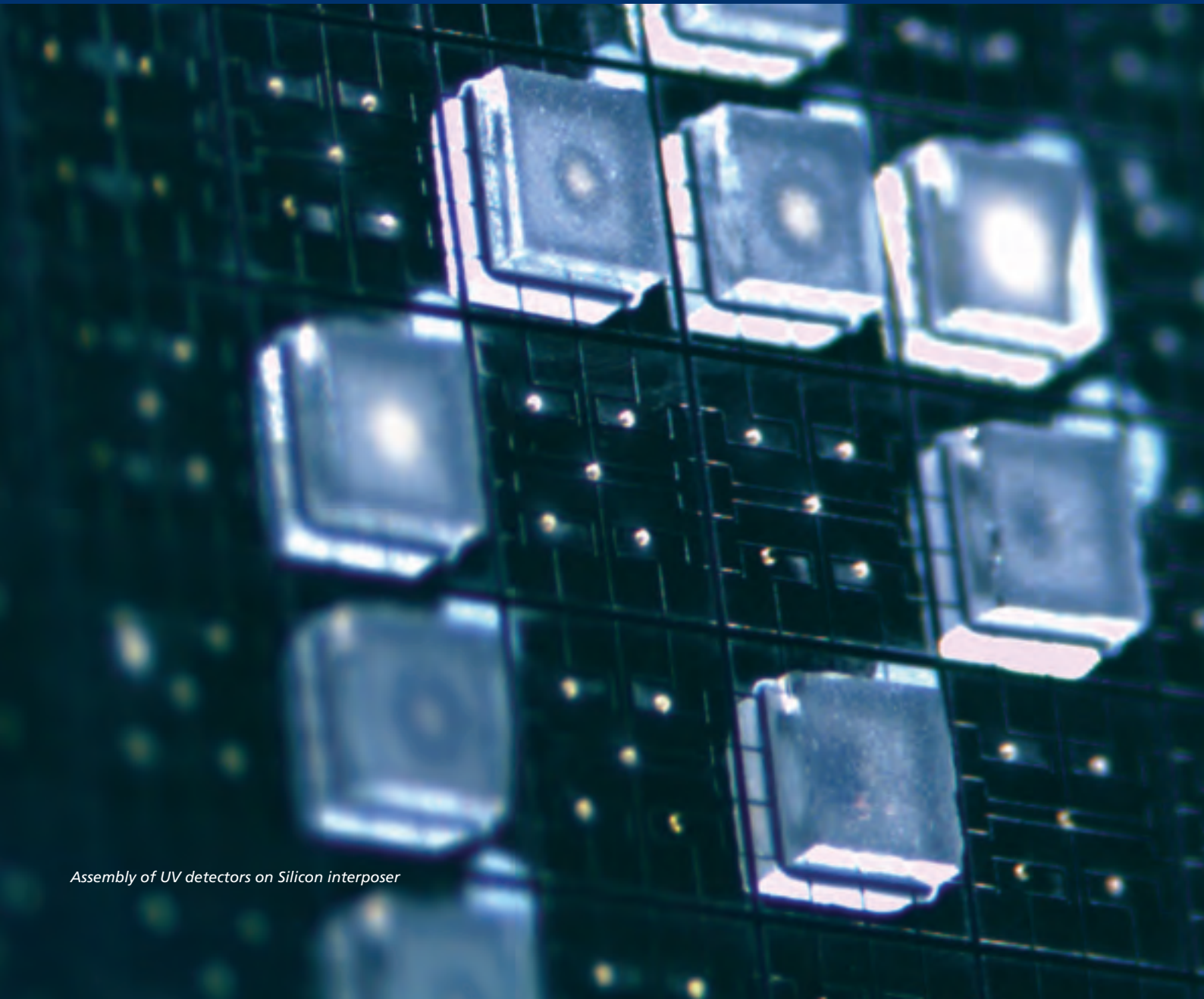
Research and Production at one Location

The Fraunhofer-Institut für Siliziumtechnologie (ISIT) develops and produces microelectronic and microsystem components. The advanced process line based on a 200 mm silicon wafer technology and the expertise built up over decades ensure a world-leading position for ISIT and its customers.

Microcomponents for a wide range of applications are developed by the institute. The main areas of application are automotive and transport engineering, consumer goods industry, medical technology, communication systems and automation. ISIT carries out the design and system simulation of microcomponents for its customers and provides samples and prototypes as well as services for series production preparation up to a pilot production.

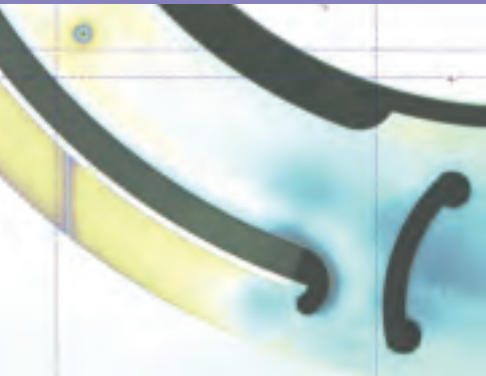
The institute also offers application-specific integrated circuits (ASICs) for the operation of sensors and actuators and deals with all the important tasks involved in system integration, assembly and interconnection technology (packaging) and the reliability and quality of components, modules and systems. The activity portfolio is completed by intensive development work on electrical energy storage devices based on Lithium polymer batteries.

MAIN FIELDS OF ACTIVITY

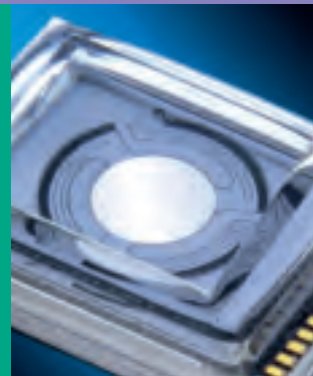


Assembly of UV detectors on Silicon interposer

MAIN FIELDS OF ACTIVITY



*Spring suspension
of a micromirror*



*Micromirror for distance
measurement*



Glass cap wafer

MICROSYSTEMS TECHNOLOGY, MEMS AND IC DESIGN

Research in microsystems technology is a major activity of Fraunhofer ISIT in different departments. For 30 years ISIT scientists are working on the development of micro electro mechanical systems (MEMS). This covers the complete development chain starting from simulation and design, technology and component development up to waferlevel probing, process qualification, and reliability tests. One of the core competences of the ISIT service offer is the development of integration technologies, like cost effective assembly of several chips in a common package, MEMS packaging on waferlevel (WLP) with defined cavity pressure or a system-on-chip approach. MEMS devices can be combined with a suitable ASIC to miniaturized systems with high functionality. ISIT has also the possibility to offer the fabrication of prototypes and a low volume pilot production. If high volume MEMS production is requested the on-site operating industrial partner X-FAB MEMS Foundry Itzehoe GmbH is able to meet this demand.

ISIT is focussed on MEMS applications in the following areas: physical sensors and actuators, devices and technologies for high frequency application (RF-MEMS), passive and active optical microsystems as well as piezoelectric MEMS.

In the field of sensor systems, strong activities are put on multi-axial inertial sensors (accelerometer, gyroscopes), magnetometers and on flow sensors. High frequency microsystems at ISIT are primarily for applications in wireless reconfigurable communication networks. In particular, developments for RF-MEMS switches, ohmic switches and waferlevel packaging are ongoing. In the field of optical MEMS devices, ISIT is active in the development of micromirrors for laser projection displays and optical measurement systems based on scanning micromirrors, e.g. LIDAR. Passive optical components based on borosilicate or quartz glass wafer processing are also in the portfolio of ISIT. Examples are glass lens arrays, aperture systems for laser beam forming and waferlevel packaging of optical MEMS.

The microsystems department operates a separate backend of line cleanroom with dedicated MEMS specific equipment and processes. The lithographic capabilities include a wide-field stepper, backside mask aligner, spray coating and thick resist processing. CVD, PVD and ALD tools for the deposition of poly-Si, SiGe, SiO₂, SiN, Ge, Au, Pt, Ir, Ag, Al, Cu, Ni, Cr, Mo, Ta, Ti, TiN, TiW, Al₂O₃, AlN, PZT and other thin films are available. The wet processing area comprises anisotropic etching of Si,



*Detail of a stepper
driver IC layout*

automated tools for metal etching and electroplating of Au, Cu and Sn. In case of dry etching, equipment for DRIE of Si and RIE of oxidic compounds is available. MEMS release etching can be performed using HF and XeF₂ gas phase etching or wet etching followed by critical point drying. A specific focus is given to hermetic waferlevel packaging of MEMS using metallic, anodic or glass frit waferbonding technology. Wafer grinding and temporary waferbonding are key process steps for thin wafer and 3D integrated products including through silicon vias. Of high importance for many MEMS, but also electronic products is the capability in chemical-mechanical polishing (CMP). The CMP application lab focusses on the development of polishing processes for Si, silicon oxides, W and Cu (damascene), and also on testing of slurries and polishing pads.

In addition to the single processes, ISIT has established a number of qualified technology platforms. Examples are the thick poly-Si surface micromachining platform for capacitive sensors/actuators and the piezoelectric MEMS platform. In the latter case sputtered thin PZT or AlN layers with suitable bottom and top electrodes are integrated in a complete process flow for piezoelectric MEMS transducers.

Beyond technology the microsystems department offers the design and realization of dedicated electronic circuits for driving/readout of the MEMS components, but also for MEMS testing and system demonstration. Moreover, an experienced ASIC design team is specialized in the design of analog/digital circuits to be integrated in smart systems. The designers also model micromechanical and micro optic elements and test their functionality in advance using FEM and behavioral modeling simulation tools. A final characterisation on wafer level or module level allows the verification of the design as well as the used technology.

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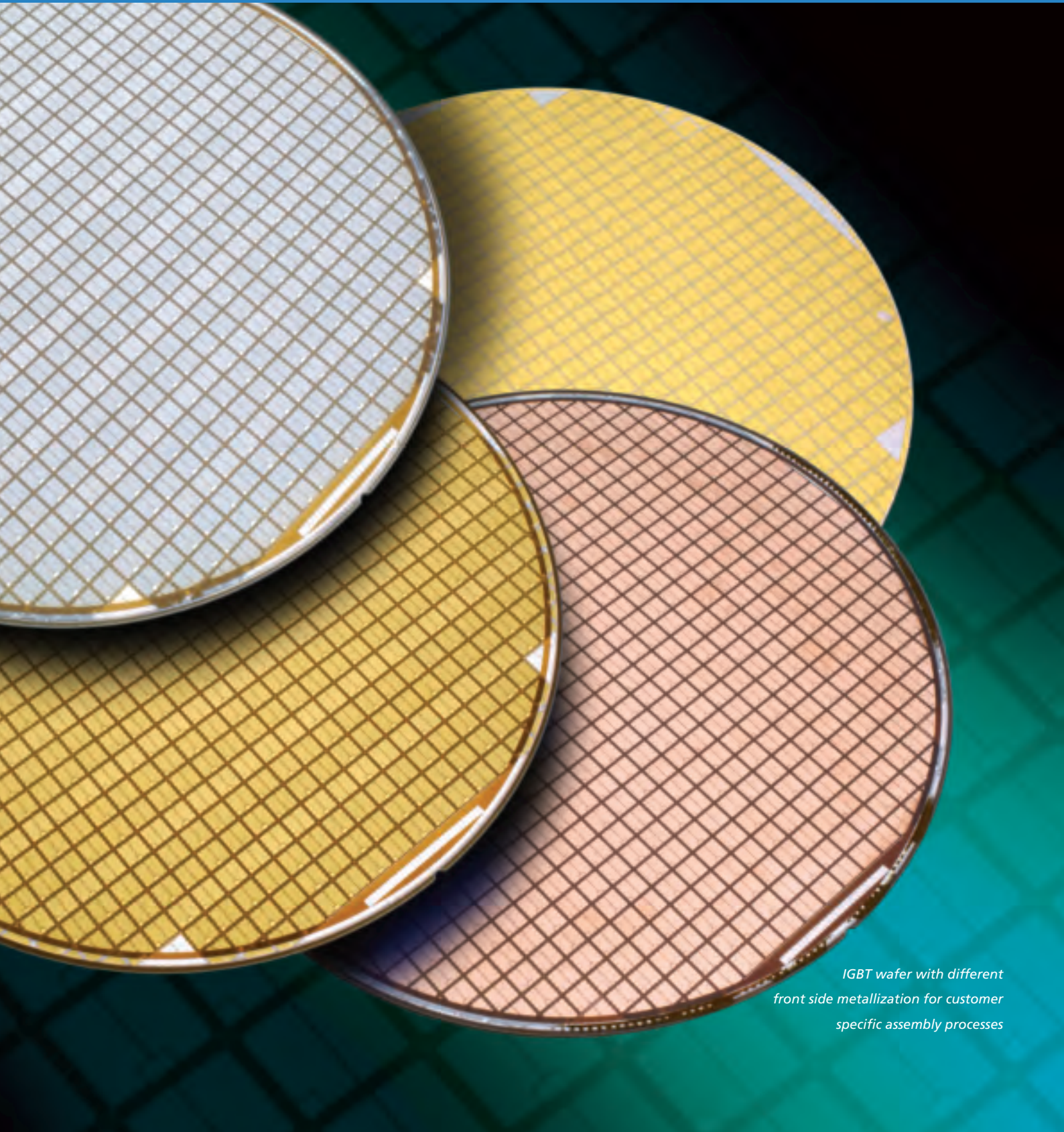
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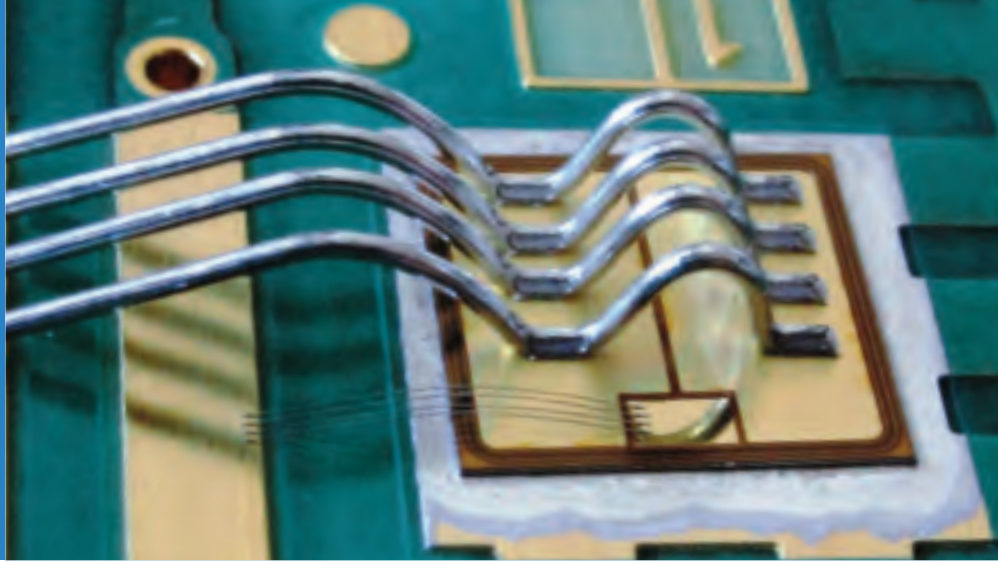
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MAIN FIELDS OF ACTIVITY



IGBT wafer with different front side metallization for customer specific assembly processes



*Wire bonded IGBT on test board
for high current characterization*

IC TECHNOLOGY AND POWER ELECTRONICS

The power electronics and IC technology group develops and manufactures active integrated circuits as well as discrete passive components.

Among the active components the emphasis lies on Silicon power devices such as smart power chips, IGBTs, PowerMOS circuits and diodes. In this context application specific power devices and new device architectures are special R&D areas. The development of new processes for advanced power device assembly on wafer level is a further important research topic. Application specific semiconductor devices with non standard metallisation layers and adapted layouts for chip geometry and pad configurations are offered for new assembly techniques. Novel techniques for backside processing of ultra thin Silicon substrates based on carrier wafer concepts and laser annealing processes are being used for power device development. Customized trade-off adjustment of static-dynamic losses and robustness are prerequisite for power electronic system optimisation and can be developed according to customer requirements.

Additional support is provided by a number of tools for simulation, design and testing. ISIT also benefits from years of experience in the design and manufacturing of CMOS circuits.

Passive components developed and fabricated at ISIT are primarily chip capacitors, precision resistors and inductors. Implementation of new materials and alloys into existing manufacturing processes is an important feature in the development process.

ISIT develops individual processes, process modules and complete process flows for diverse applications. The institute also offers processing of customer specific silicon components in small to medium sized quantities on the basis of a qualified semiconductor process technology.

A special R&D group with focus on power electronic systems works on application specific topics covering the interface to system end users. New circuit topologies based on system specific semiconductor power devices are special R&D topics for system optimisation.

In the field of power electronics ISIT coordinates a competence centre which was founded in close cooperation with universities and companies of the federal country Schleswig-Holstein. In this context an Innovation Cluster for power electronics of renewable energy supply has been initiated.

IC Technology and Power Electronics

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Portable food analysis system



Electrical connected membrane sensor chip in a flow through reaction compartment

BIOTECHNICAL MICROSYSTEMS

ISIT is one of the worldwide leaders at the field of electrical biochips. These chips allow the realization of very efficient biosensors and are the basis for fast and cost effective analytical systems.

The electrical biochip technology offers intrinsic advantages over optical biochips because of particle tolerance and mechanical robustness by the direct transduction of biochemical reactions into electrical current. The use of gold electrode arrays combined with integrated reference and auxiliary electrodes along with sensitive, selective measurement techniques like "Redox-Cycling" enables powerful sensor systems. These arrays are useful for the detection of a variety of analytes within one probe simultaneously. User-friendly operability is realized by integrating the biochips into cartridges. In combination with micro-fluidic components and integrated electronics, these electrical microarrays represent the basis of rapid and cost-effective analysis systems. They can be used to identify and quantify DNA, RNA and proteins. Further biosensors enable continuous monitoring, e.g. of metabolites as glucose or lactate. The measurement of these substances is realized by enzymatic conversion and electrochemical detection.

The development of additional micro systems for specialized applications involves the production of different kinds of modified electrodes. Supplementary to gold and platinum, diamond electrodes show intrinsic advantages in direct electrochemical detection of substances, e.g. in pulsed amperometry. They are suitable for the detection in chromatography applications (e.g. HPLC) and can be integrated in miniaturized systems like a MEMS chromatography chip.

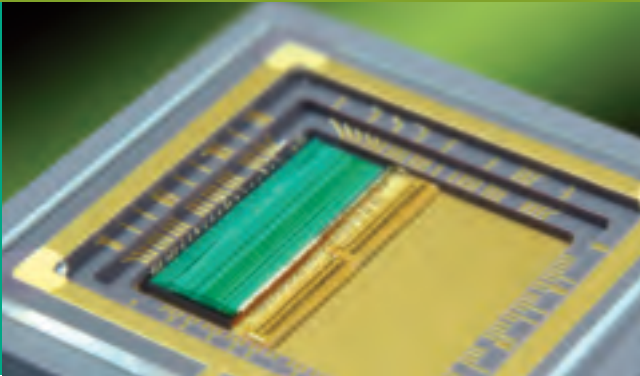
Biotechnical Microsystems

Dr. Eric Nebling

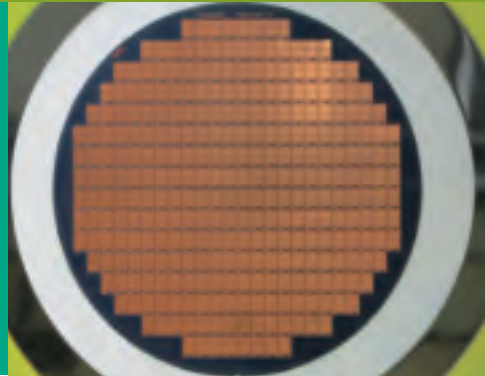
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Miniaturized iridium oxide electrode chips are used for potentiometric measurements in small volume flow through cells and bio reactors.



*Two UV sensitive line detectors
with read out circuit*



*Testwafer for copper
ribbon bonding*

PACKAGING TECHNOLOGY FOR MICROELECTRONICS AND MICROSYSTEMS

The "Advanced Packaging" group is specialized in detecting and promoting new trends and technologies in electronics packaging. The industrial challenges of tomorrow are addressed in direct collaboration with suppliers of materials, components, modules and equipment.

As an example, the automatic assembly of thin dies on flexible substrates was already developed several years ago. For the encapsulation of MEMS components, the glass frit bonding was developed and later on replaced by the more efficient metallic bonding. ISIT equally participates in development activities on flexible electronics and RFID technology. Moreover new digital techniques like functional inkjet printing offer new degrees of freedom in assembly and integration of electronic modules and systems.

The Fraunhofer ISIT disposes of all basic technologies for the automatic or manual handling of microchips and microsensors, as well as electrical interconnect methods like wire bonding and flip chip technologies. Through the close relationship between MEMS technology and packaging in ISIT's premises, the institute has become a leading R&D service provider in the domain of waferlevel packaging. A cross-disciplinary technology portfolio is now available that allows to reduce cost and volume of a system. Even more, the packaging itself can become a functional part of the microsystem in many cases, e.g. by integrating optical elements or directly interconnecting MEMS and ASIC dies. Outstanding success was achieved in the vacuum encapsulation of micromechanical sensors by eutectic wafer bonding, which paved the way towards the industrialisation of a gyro sensor product family for automotive applications.

ISIT continuously expands their assortment of test chips and -substrates that facilitate the ramp up and calibration of production lines for securing quality on a high level.

*Packaging Technology for Micro-
electronics and Microsystems*

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*Sample mount on a glass rod
for CT analysis*

QUALITY AND RELIABILITY OF ELECTRONIC ASSEMBLIES

Quality evaluation – in particular for the soldering work done in pre-production, pilot and main series lots – represents a continuous challenge for ISIT, as for example whenever new technologies such as lead-free soldering are introduced, or when increased error rates are discovered, or if a customer desires to achieve competitive advantages through continual product improvement. To reveal potential weak points, ISIT employs both destructive and non-destructive analysis methods, such as X-ray transmission radiography, computer tomography, laser profilometry and scanning acoustic microscopy. Working from a requirements matrix, ISIT scientists also evaluate long-term behavior of lead-free and lead-containing assemblies alike. They then formulate prognoses on the basis of model calculations, environmental and time-lapse load tests, and failure analysis.

In anticipation of a conversion to lead-free electronics manufacturing, Fraunhofer ISIT is undertaking design, material selection and process modification projects for industrial partners. To effect a further optimization of manufacturing processes, the institute applies process models and produces samples on industry-compatible equipment. The group also addresses issues related to thermal management and reliability for customer-specific power modules.

In addition to these technological activities, the group regularly holds training sessions, including multi-day classes, at the institute or at company site.

*Quality and Reliability of
Electronic Assemblies*

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*Manufactured electrode foils for
Lithium polymer batteries*



*Electrode stack of anode,
separator and cathode*

INTEGRATED POWER SYSTEMS

Secondary Lithium batteries as a powerful storage medium for electrical energy are rapidly capturing new fields of application outside of the market of portable electronic equipment.

These new fields include automobiles, medical devices, stationary electric storage units, aerospace, etc. Therefore, this type of rechargeable batteries has to meet a variety of new requirements. This covers not only electrical performance but also design and safety features. The Lithium polymer technology developed at ISIT is characterized by an extensive adaptability to specific application profiles like extended temperature range, high power rating, long shelf and/or cycle life, extended safety requirements, etc (tailor-made, energy storage solutions). Also included is the development of application-specific housings.

In the Lithium polymer technology all components of the cell from electrodes to housing are made from tapes. At ISIT the complete process chain starting with the slurry preparation over the tape casting process and the assembly and packaging of complete cells in customized designs is available including also the electrical and thermo-mechanical characterization. This allows access to all relevant parameters necessary for an optimization process. The electrode and the electrolyte composition up to the cell design can be modified.

In addition to the development of prototypes, limited-lot manufacturing of optimized cells on a pilot production line at ISIT with storage capacities of up to several ampere-hours is possible. Specific consideration in process development is addressed to the transferability of development results in a subsequent industrial production.

ISIT offers a wide portfolio of services in the field of secondary Lithium batteries:

- Manufacturing and characterization of battery raw materials by half cell as well as full cell testing
- Selection of appropriate combinations of materials and design of cells to fulfil customer requirements
- Application driven housing development
- Test panel
- Prototyping and limited-lot manufacturing of cells

Additional services are:

- Preparation of studies
- Failure analysis
- Testing (electrical, mechanical, reliability etc.)
- Technical consultation

Integrated Power Systems

Dr. Peter Gulde

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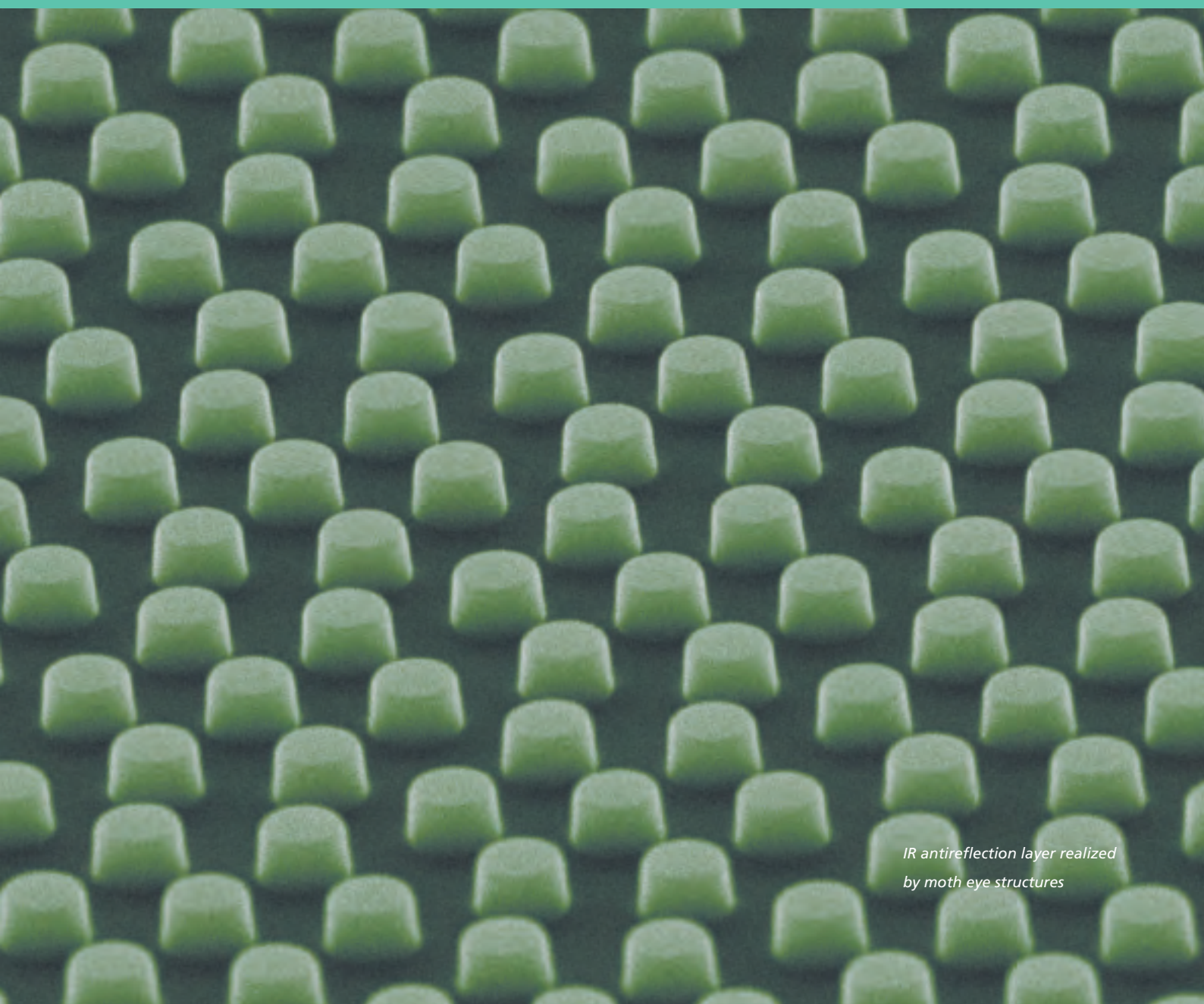
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OFFERS FOR RESEARCH AND SERVICE



*IR antireflection layer realized
by moth eye structures*



CT X-ray inspection system at ISIT

FACILITIES AND EQUIPMENT

ISIT operates in collaboration with Vishay Siliconix Itzehoe GmbH a semiconductor production line for 200 mm (8") Si wafers (cleanroom area 2.500 m²). The process line is used for the development of new components and processes as well as for the production of components (PowerMOS, MEMS). Further cleanrooms (650 m²) are available for specific processes, as needed for example in microsystem engineering, and for chemical-mechanical polishing (CMP). In addition to the basic processes of microsystem engineering, highly developed processes are maintained, e.g. for high-precision deep etching (DRIE), deposition of non-IC-compatible materials such as piezoelectrics, thick-layer lithography and electroplating, glass molding and grey-scale lithography.

The institute has particular expertise in wafer bonding and waferlevel packaging (WLP), achieving unique levels of quality for various MEMS components (gyroscopes, scanner mirrors, RF-MEMS, etc.). Further laboratory areas (1.500 m²) are equipped for characterization, qualification and assembly and interconnection technology. The scope of activities is widened by laboratories for the development of Lithium polymer batteries, in which a pilot production plant is operated for sample production and evaluation tasks. To expand the institute's capacity, a further cleanroom and laboratory building is presently under construction. The completion is scheduled for mid 2013. The ISIT's facilities are certified to ISO 9001-2008.

RANGE OF SERVICES

Fraunhofer ISIT has many years of experience in industrial collaboration. Primarily the concept of technology platforms is pursued, i.e. the definition of process procedures in which the customer-specific solutions take place through the design and packaging. This allows to offer services which, beyond the technical specifications, are attractive in terms of risk, development time, development expense and production cost. Series production can ultimately be carried out in close cooperation with the locally based X-FAB MEMS Foundry Itzehoe GmbH.

CUSTOMERS

ISIT cooperates with companies of different sectors and sizes. In the following, some companies are presented as a reference:



ABB AG, Ladenburg

Advaplan, Espoo, Finland

Air Liquide GmbH, Stade

Airbus-Systeme, Buxtehude

aixACCT Systems GmbH, Aachen

ams AG, Unterpremstätten, Austria

Analytik Jena AG, Jena

Andus electronic GmbH, Berlin

Atotech Deutschland GmbH, Berlin

BASF SE, Ludwigshafen

Basler Vision Technologies, Ahrensburg

Besi Austria GmbH, Radfeld, Austria

Besi APac Sdn. Bhd., Malaysia

BMW AG, München

BMW Forschung und Technik GmbH, München

Bosch Sensortec GmbH, Reutlingen

B. Braun, Melsungen

CAPRES A/S, Kongens Lyngby, Denmark

CarboFibretec GmbH, Friedrichshafen

Cassidian Electronics, Ulm

Condias GmbH, Itzehoe

Conti Temic, Karben

Conti Temic microelectronic GmbH, Nürnberg

Continental, Nürnberg

CS Energy Materials GmbH, Goslar

Danfoss Drives, Graasten, Denmark

Danfoss Silicon Power GmbH, Schleswig

davengo GmbH, Berlin

Diehl Avionik Systeme GmbH, Überlingen

Dispatch Energy Innovations GmbH, Itzehoe

Dow Chemical Company, Lausanne, Switzerland

Dräger Systemtechnik, Lübeck

E.G.O. Elektro-Gerätebau GmbH, Oberderdingen

EADS Deutschland GmbH, Corporate Research Germany, München and Ulm

EN Electronic Network, Bad Hersfeld

Endress + Hauser GmbH Co. KG, Maulburg

Engineering Center for Power Electronics GmbH, Nürnberg

EPCOS, Nijmegen, Netherlands

EPCOS AG, München

Ernemann CineTec GmbH, Kiel

ESCD, Brunsbüttel

ESPROS Photonics AG, Schweiz

ESW-Extel Systems GmbH, Wedel

EVGroup, Schärding, Austria

Evonik Degussa GmbH, Hanau

Freudenberg & Co. KG, Weinheim

Fujitsu Siemens Computers GmbH, Augsburg

GEMALTO, Meudon, France

GÖPEL electronic GmbH, Jena

Hako-Werke, Bad Oldesloe

Hannusc Industrieelektronik, Laichingen

Harman & Becker, Karlsbad

Hella KG, Lippstadt

Heraus Materials Technology GmbH Co. KG, Hanau

Honeywell Deutschland AG, Offenbach

HSG-IMIT, Villingen-Schwenningen

Ifm electronic GmbH, Essen

IMS Nanofabrication AG, Wien, Austria

Isola GmbH, Düren

Jenoptik ESW GmbH, Essen

Jenoptik InnovaVent GmbH, Göttingen

Johnson & Johnson Medical GmbH, Norderstedt

Jungheinrich AG, Norderstedt

Kristronics GmbH, Harrislee-Flensburg

Kuhnke GmbH, Malente

Lam Research, Fremont, USA

Lenze Drive Systems GmbH, Hameln

Lenze Operations GmbH, Aerzen

Limedion GmbH, Mannheim

Liebherr Elektronik, Lindau

Litef, Freiburg

LPKF AG, Garbsen

Mair Elektronik GmbH, Neufahrn

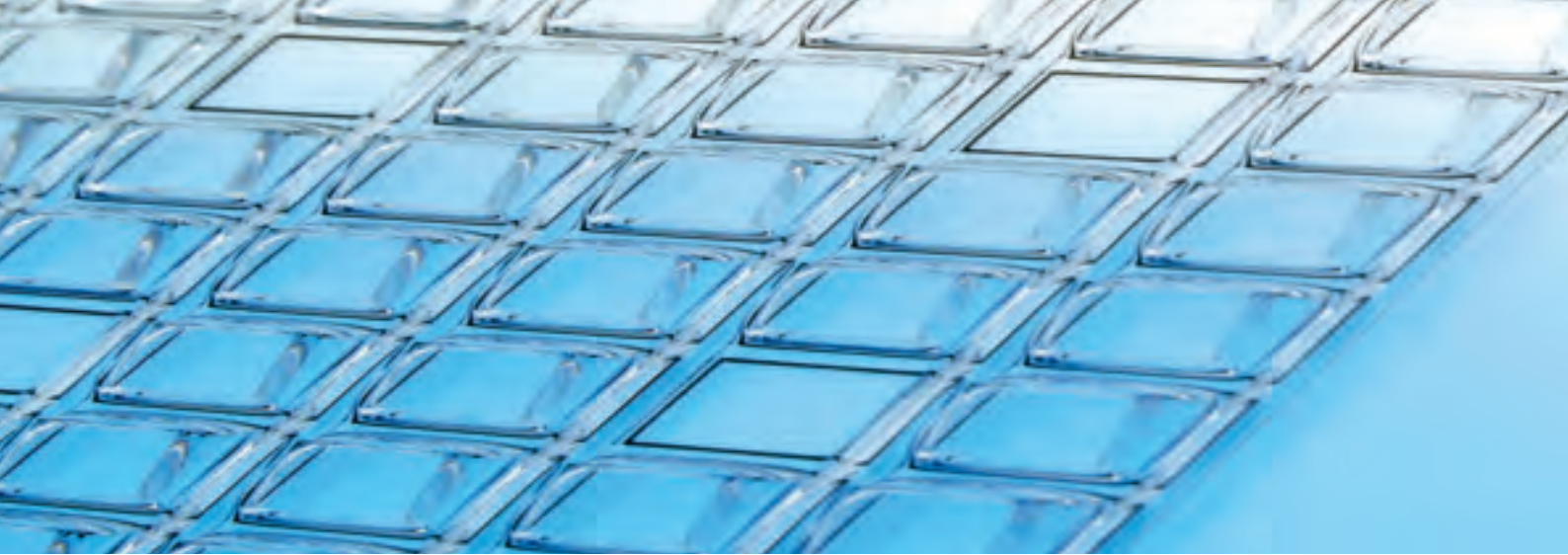
Manz AG, Reutlingen

Marquardt, Rietheim-Weilheim

MASER Engineering B.V., Enschede, Netherlands

Maxim Integrated Products Inc., Oberkochen

Maxim Integrated GmbH, Lebring, Austria



Meder electronic AG,
Engen-Welschingen

Melexis Ieper N.V., *Belgium*

Micropelt GmbH, *Freiburg*

MKS, *München*

mut AG, *Wedel*

NEXT VIDEO SYSTEMS,
Neumünster

NXP Semiconductors,
Hamburg

Océ-Technologies B.V.,
Venlo, Netherlands

Oerlikon AG, *Liechtenstein*

Okmetic Oyj, *Vantaa,*
Finland

OMT/ECC GmbH, *Lübeck*

Osram GmbH, *München*

Osram Opto Semiconductors
GmbH, *Regensburg*

Otto Bock HealthCare
GmbH, *Duderstadt*

Pac Tech, Packaging
Technologies,
Santa Clara, USA

Panasonic, *Neumünster*

PAV Card GmbH, *Lütjensee*

Peter Wolters GmbH,
Rendsburg

Picosun Oy, *Espoo, Finland*

PlanOptik AG, *Elsoff*

Plath Eft GmbH, *Norderstedt*

POCDIA GmbH, *Itzehoe*

Prettl Elektronik Lübeck
GmbH, *Lübeck*

Raytheon Anschütz GmbH,
Kiel

Reese und Thies, *Itzehoe*

RefuSol GmbH, *Metzingen*

Rehm Anlagenbau GmbH,
Blaubeuren-Seissen

Rena Sondermaschinen
GmbH, *Gütenbach*

REpower Systems SE,
Osterröhnfeld

Robert Bosch GmbH,
Reutlingen

Robert Bosch GmbH,
Salzgitter

Robert Bosch GmbH,
Stuttgart

ROFIN-BAASEL Lasertech
GmbH Co. KG, *Starnberg*

SAES Getters S.p.A.,
Lainate/Milan, Italy

Sartorius Hamburg GmbH
Research & Development,
Hamburg

Sauer, Danfoss,
Nordborg, Denmark

SEF GmbH, *Scharnebek*

Sensoror Technologies AS,
Horten, Norway

Silex Microsystems AG,
Järfälla, Sweden

SMA Regelsysteme GmbH,
Niestetal

Smart Material GmbH,
Dresden

Smyczek, *Verl*

Solar Direct GmbH, *Itzehoe*

SolMateS B.V., *Enschede,*
Netherlands

Spheros GmbH, *Gilching*

STABILO International
GmbH, *Heroldsberg*

Sterling Industry Consult
GmbH, *Itzehoe*

Still GmbH, *Hamburg*

SÜSS Microtec AG, *Garching*

tagitron GmbH, *Salzkotten*

Technolas, *München*

Theon, *Athens, Greece*

Trainalytics GmbH, *Lippstadt*

Treichel Elektronik GmbH,
Springe

Trinamic, *Hamburg*

Umicore AG & Co., *Hanau*

Vectron International
GmbH & Co. KG,
Neckarbischofsheim

Vishay BCcomponents
Beyschlag GmbH,
Heide

Vishay Siliconix Itzehoe
GmbH, *Itzehoe*

Vishay Siliconix, *Santa Clara,*
USA

Vistec, *Jena*

Volkswagen AG, *Wolfsburg*

Wabco Fahrzeugbremsen,
Hannover

Würth Elektronik GmbH,
Schopfheim

X-FAB MEMS Foundry
Itzehoe GmbH, *Itzehoe*

X-FAB Semiconductor
Foundries AG, *Erfurt*

Carl Zeiss SMT GmbH,
Oberkochen

Vishay Siliconix,
Santa Clara, USA

Vistec, *Jena*

Volkswagen AG, *Wolfsburg*

Wabco Fahrzeugbremsen,
Hannover

Würth Elektronik GmbH,
Schopfheim

INNOVATION CATALOGUE

ISIT offers its customers various products and services already developed for market introduction. The following table presents a summary of the essential products and services. Beyond that the utilisation of patents and licences is included in the service..

Product / Service	Market	Contact Person
Testing of semiconductor manufacturing equipment	Semiconductor equipment manufacturers	Dr. Gerfried Zwicker + 49 (0) 4821/17-4309 gerfried.zwicker@isit.fraunhofer.de
Chemical-mechanical polishing (CMP), planarization	Semiconductor device manufacturers	Dr. Gerfried Zwicker + 49 (0) 4821/17-4309 gerfried.zwicker@isit.fraunhofer.de
Wafer polishing	Si substrates for device manufacturers	Dr. Gerfried Zwicker + 49 (0) 4821/17-4309 gerfried.zwicker@isit.fraunhofer.de
IC processes and power devices CMOS, PowerMOS, IGBTs	Semiconductor industry IC-users	Detlef Friedrich + 49 (0) 4821/17-4301 detlef.friedrich@isit.fraunhofer.de
Single processes and process module development	Semiconductor industry semiconductor equipment manufacturers	Detlef Friedrich + 49 (0) 4821/17-4301 detlef.friedrich@isit.fraunhofer.de
Customer specific processing	Semiconductor industry semiconductor equipment manufacturers	Detlef Friedrich + 49 (0) 4821/17-4301 detlef.friedrich@isit.fraunhofer.de
Microsystem products	Electronic industry	Prof. Ralf Dudde + 49 (0) 4821/17-4212 ralf.dudde@isit.fraunhofer.de
MEMS process Development and Integration	Electronic industry	Christian Schröder + 49 (0) 4821/17-4232 christian.schroeder@isit.fraunhofer.de
Inertial sensors	Motorvehicle technology, navigation systems, measurements	Dr. Klaus Reimer + 49 (0) 4821/17-4213 klaus.reimer@isit.fraunhofer.de
Piezoelectric microsystems	Sensors and actuators	Hans-Joachim Quenzer + 49 (0) 4821/17-4643 hans-joachim.quenzer@isit.fraunhofer.de
Microoptical scanners and projectors	Biomedical technology, optical measurement industry, telecommunication	Ulrich Hofmann + 49 (0) 4821/17-4553 ulrich.hofmann@isit.fraunhofer.de
Flow sensors	Automotive, fuel cells	Dr. Peter Lange +49 (0) 4821/17-4506 peter.lange@isit.fraunhofer.de
Microoptical components	Optical measurement	Hans-Joachim Quenzer + 49 (0) 4821/17-4643 hans-joachim.quenzer@isit.fraunhofer.de
RF-MEMS	Telecommunication	Dr. Thomas Lisec + 49 (0) 4821/17-4512 thomas.lisec@isit.fraunhofer.de
Beam deflection components for maskless nanolithography	Semiconductor equipment manufacturers	Dr. Klaus Reimer + 49 (0) 4821/17-4233 klaus.reimer@isit.fraunhofer.de

Product / Service	Market	Contact Person
<i>Design and test of analogue and mixed-signal ASICs</i>	<i>Measurement, automatic control industry</i>	Jörg Eichholz + 49 (0) 4821/17-4253 joerg.eichholz@isit.fraunhofer.de
<i>Design Kits</i>	<i>MST foundries</i>	Jörg Eichholz + 49 (0) 4821/17-4253 joerg.eichholz@isit.fraunhofer.de
<i>MST design and behavioural modelling and wafer tests</i>	<i>Measurement, automatic control industry</i>	Jörg Eichholz + 49 (0) 4821/17-4253 joerg.eichholz@isit.fraunhofer.de
<i>Electrodeposition of microstructures</i>	<i>Surface micromachining</i>	Martin Witt + 49 (0) 4821/17-4613 martin.witt@isit.fraunhofer.de
<i>Electrical biochip technology (proteins, nucleic acids, haptens)</i>	<i>Biotechnology, related electronics microfluidics, environmental analysis, Si-Chip processing, packaging, chip loading</i>	Dr. Eric Nebling + 49 (0) 4821/17-4312 eric.nebling@isit.fraunhofer.de
<i>Secondary lithium batteries</i>	<i>Mobile electronic equipment, medical applications, automotive, smart cards, labels, tags</i>	Dr. Peter Gulde +49 (0) 4821/17-4219 peter.gulde@isit.fraunhofer.de
<i>Battery test service, electrical parameters, climate impact, reliability, quality</i>	<i>Mobile electronic equipment, medical applications, stationary storage solutions, automotive, smart cards labels, tags</i>	Dr. Peter Gulde +49 (0) 4821/17-4219 peter.gulde@isit.fraunhofer.de
<i>Quality and reliability of electronic assemblies</i>	<i>Microelectronic and power electronic industry</i>	Karin Pape + 49 (0) 4821/17-4229 karin.pape@isit.fraunhofer.de
<i>Material and damage analysis</i>	<i>Microelectronic and power electronic industry</i>	Dr. Thomas Knieling + 49 (0) 4821/17-4605 thomas.knieling@isit.fraunhofer.de
<i>Printed Electronics</i>	<i>Electronic Industry</i>	Dr. Thomas Knieling + 49 (0) 4821/17-4605 thomas.knieling@isit.fraunhofer.de
<i>Thermal measurement and simulation</i>	<i>Microelectronic and power electronic industry</i>	Dr. M. H. Poech + 49 (0) 4821/17-4607 max.poech@isit.fraunhofer.de
<i>Leadfree / RoHS transformation in electronic assembly</i>	<i>Electronic industry</i>	Helge Schimanski +49 (0) 4821/17-4639 helge.schimanski@isit.fraunhofer.de
<i>Packaging for microsystems, sensors, multichip modules</i>	<i>Microelectronic, sensoric and medical industry</i>	Karin Pape + 49 (0) 4821/17-4229 karin.pape@isit.fraunhofer.de
<i>Wafer level packaging, ultra thin Si packaging and direct chip attach techniques</i>	<i>Microelectronic, sensoric and medical industry, automotive industry</i>	Dr. Wolfgang Reinert + 49 (0) 4821/17-4617 wolfgang.reinert@isit.fraunhofer.de
<i>Vacuum wafer bonding technology</i>	<i>Microelectronic, sensoric and medical industry, automotive industry</i>	Dr. Wolfgang Reinert + 49 (0) 4821/17-4617 wolfgang.reinert@isit.fraunhofer.de

REPRESENTATIVE FIGURES

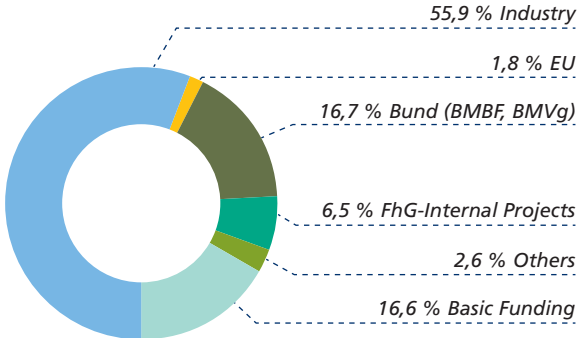
EXPENDITURE

In 2012 the operating expenditure of Fraunhofer ISIT amounted to 22.328,7 T€. Salaries and wages were 9.177,7 T€, material costs and different other running costs were 11.880,0 T€. The institutional budget of capital investment was 1.271,1 T€.

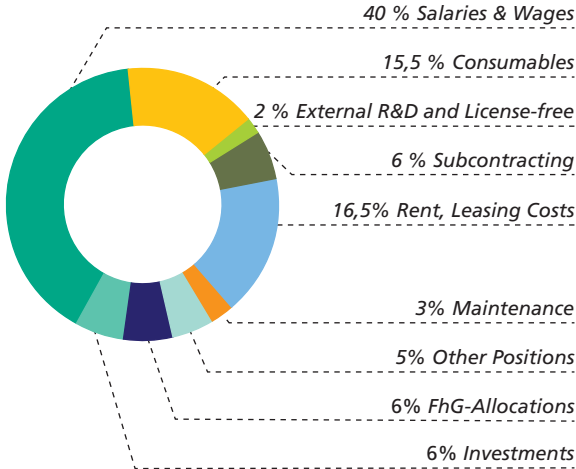
INCOME

The budget was financed by proceeds of projects of industry/industrial federations / small and medium sized companies amounting to 12.476,2 T€, of government / project sponsors /federal states amounting to 3.719,4 T€ and of European Union /others amounting to 973,5 T€. Furthermore there were FhG-projects about 1.458,0 T€ and basic funding with 3.701,6 T€.

Income



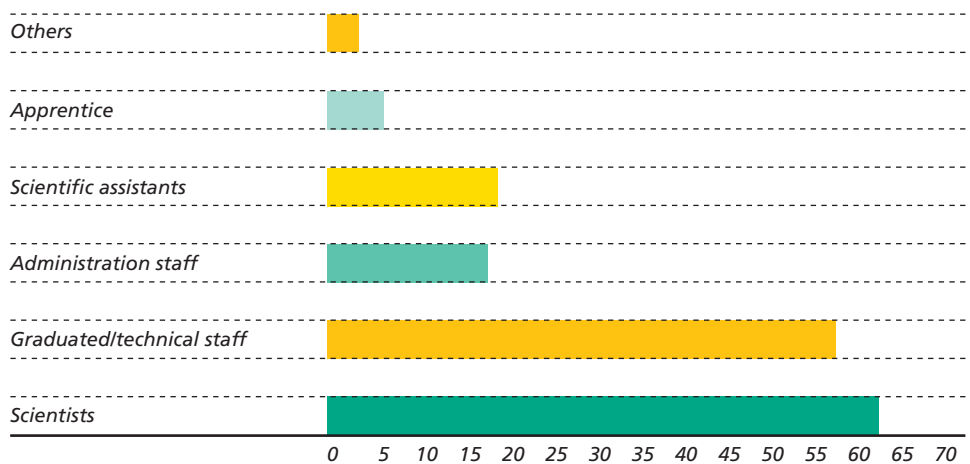
Expenditure



STAFF DEVELOPMENT

In 2012, on annual average, the staff consisted of 135 employees. 62 were employed as scientific personnel, 57 as graduated / technical personnel and 16 worked within organisation and administration. The employees were assisted through 17 scientific assistants, 5 apprentices and 3 others.

Staff Development



THE FRAUNHOFER-GESELLSCHAFT

Research of practical utility lies at the heart of all activities pursued by the Fraunhofer-Gesellschaft. Founded in 1949, the research organization undertakes applied research that drives economic development and serves the wider benefit of society. Its services are solicited by customers and contractual partners in industry, the service sector and public administration.

At present, the Fraunhofer-Gesellschaft maintains 66 institutes and independent research units. The majority of the more than 22,000 staff are qualified scientists and engineers, who work with an annual research budget of 1.9 billion euros. Of this sum, more than 1.6 billion euros is generated through contract research. More than 70 percent of the Fraunhofer-Gesellschaft's contract research revenue is derived from contracts with industry and from publicly financed research projects. Almost 30 percent is contributed by the German federal and Länder governments in the form of base funding, enabling the institutes to work ahead on solutions to problems that will not become acutely relevant to industry and society until five or ten years from now.

Affiliated international research centers and representative offices provide contact with the regions of greatest importance to present and future scientific progress and economic development.

With its clearly defined mission of application-oriented research and its focus on key technologies of relevance to the future, the Fraunhofer-Gesellschaft plays a prominent role in the German and European innovation process. Applied

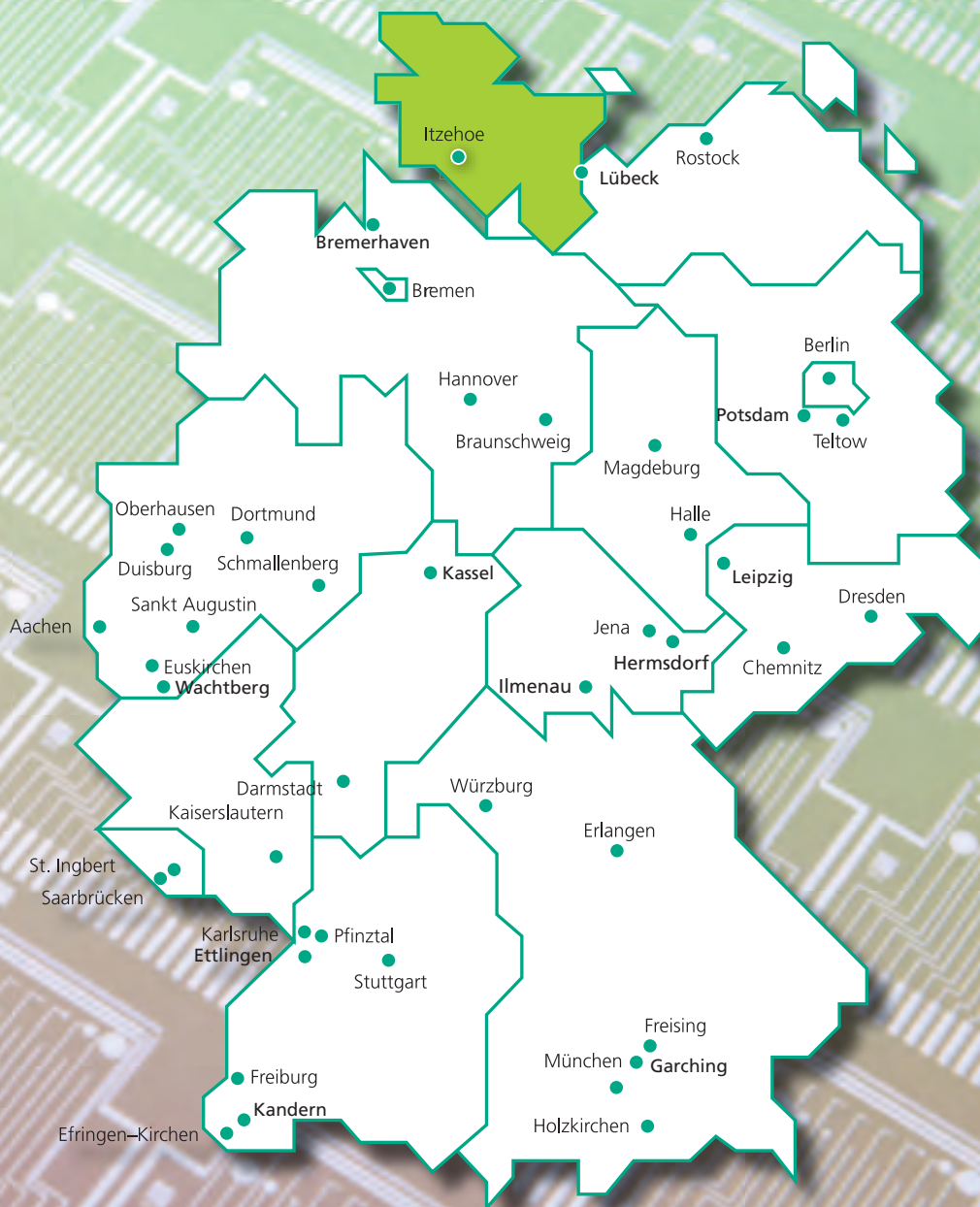
research has a knock-on effect that extends beyond the direct benefits perceived by the customer: Through their research and development work, the Fraunhofer Institutes help to reinforce the competitive strength of the economy in their local region, and throughout Germany and Europe. They do so by promoting innovation, strengthening the technological base, improving the acceptance of new technologies, and helping to train the urgently needed future generation of scientists and engineers.

As an employer, the Fraunhofer-Gesellschaft offers its staff the opportunity to develop the professional and personal skills that will allow them to take up positions of responsibility within their institute, at universities, in industry and in society. Students who choose to work on projects at the Fraunhofer Institutes have excellent prospects of starting and developing a career in industry by virtue of the practical training and experience they have acquired.

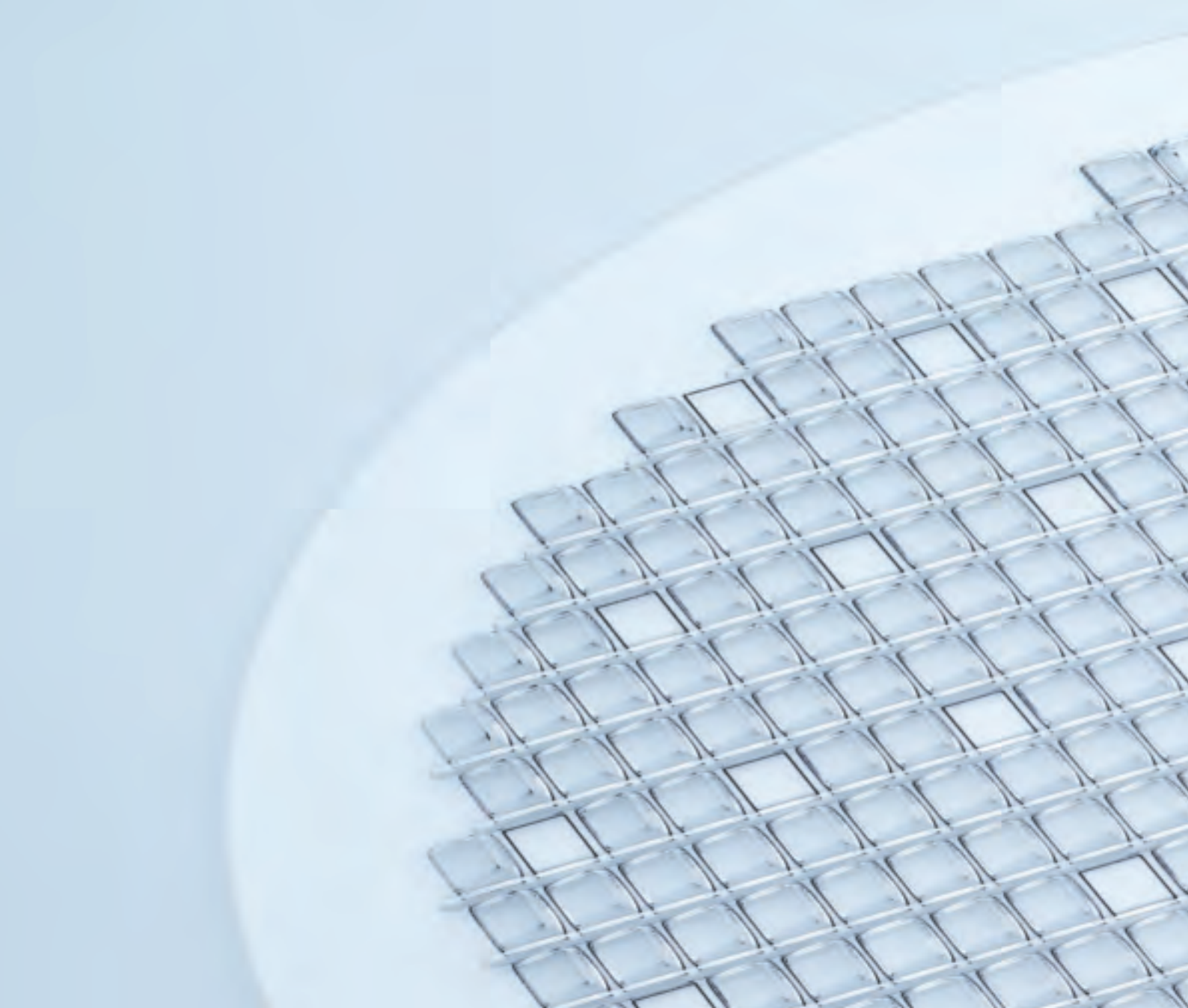
The Fraunhofer-Gesellschaft is a recognized non-profit organization that takes its name from Joseph von Fraunhofer (1787–1826), the illustrious Munich researcher, inventor and entrepreneur.

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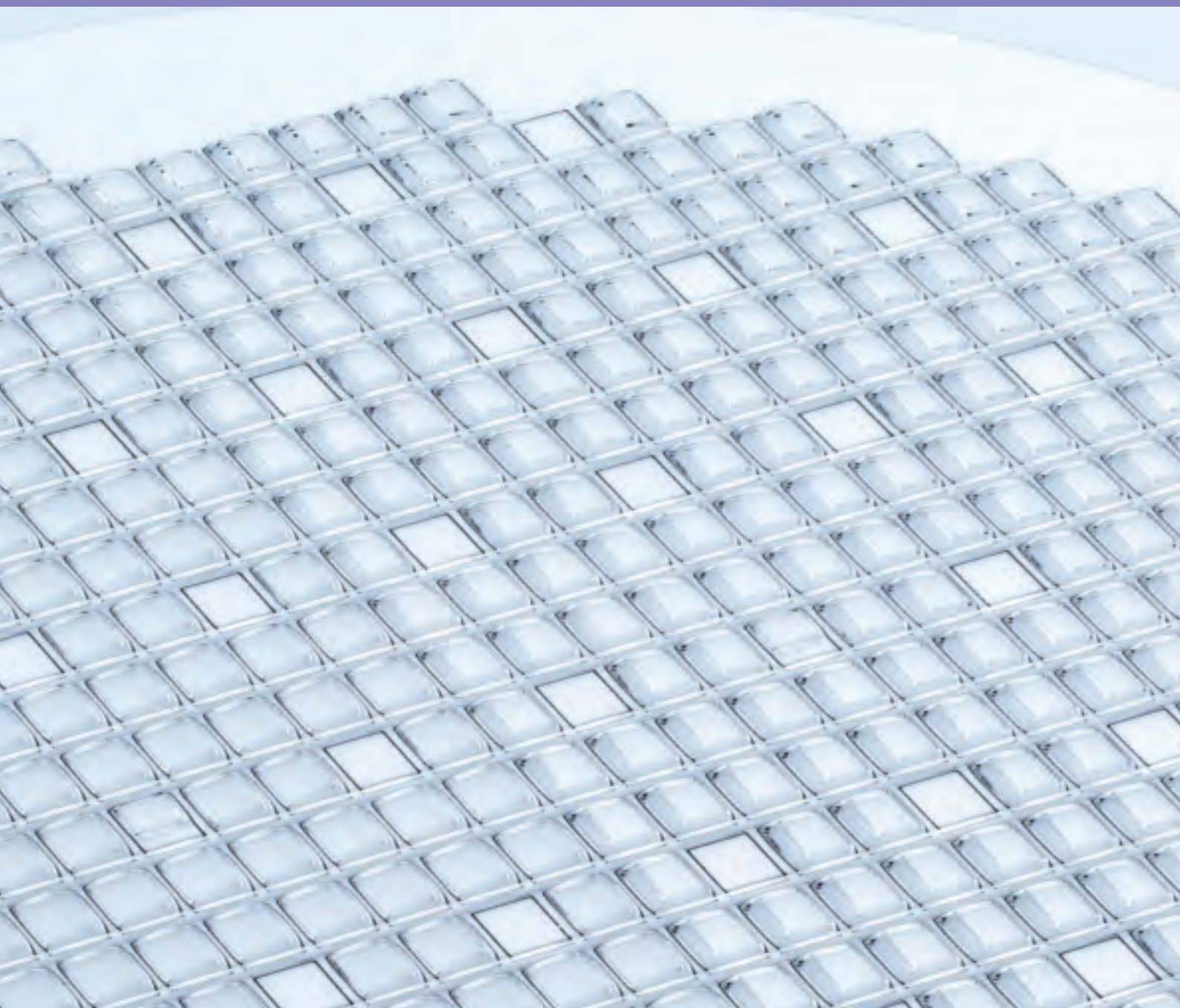
LOCATIONS OF THE RESEARCH ESTABLISHMENT



REPRESENTATIVE RESULTS OF WORK



**MICROSYSTEMS TECHNOLOGY,
MEMS AND IC DESIGN**



RESONANT BIAxIAL 7-MM MEMS MIRROR FOR OMNIDIRECTIONAL SCANNING

There are over one million traffic accidents on European roads every year causing more than 30 thousand fatalities. In order to seriously reduce the number of traffic accidents, Intelligent Vehicle Safety Systems (IVSS) need to be introduced into all vehicle segments. Today, IVSS are limited to a very small part of the premium car segment only. However, statistics show that in more than 80% of all traffic accidents either subcompact cars, compact cars or midsize cars are involved. For that reason, safety systems must be made affordable to penetrate all vehicle segments, since small and medium size cars are the ones dominating the road traffic and thus most of the accidents.

These figures show a large market potential of low cost laser scanning sensors for reliable detection of the host vehicle's surrounding. Such sensor functionality is the basis for Intelligent Vehicle Safety Systems and can help for instance to protect pedestrians in right-turn situations of trucks, or inhibit

the start of a truck if pedestrians cross directly in front of the vehicle out of the driver's field of view. Other systems assist by keeping the car at safe distance to preceding vehicles and help avoiding collisions.

Within the European funded project MiniFaros, Fraunhofer ISIT cooperated with partners from five different countries in developing a small sized low-cost time-of-flight based laser range sensor for detection of pedestrians, cyclists, cars, trucks and obstacles. A wide angular range and high angular resolution are key features that laser scanning range sensors can offer. But so far they have been based on expensive and bulky servo motor driven scanning mirrors. Thus, it has been one of the major objectives of the MiniFaros project to replace the expensive conventional scanning mirror by a low cost, mass producible MEMS mirror. To support many different IVSS applications, an optical scanning concept was chosen that provides

Figure 1: Omnidirectional scanning concept based on omnidirectional lens and Fraunhofer ISIT's biaxial MEMS-mirror

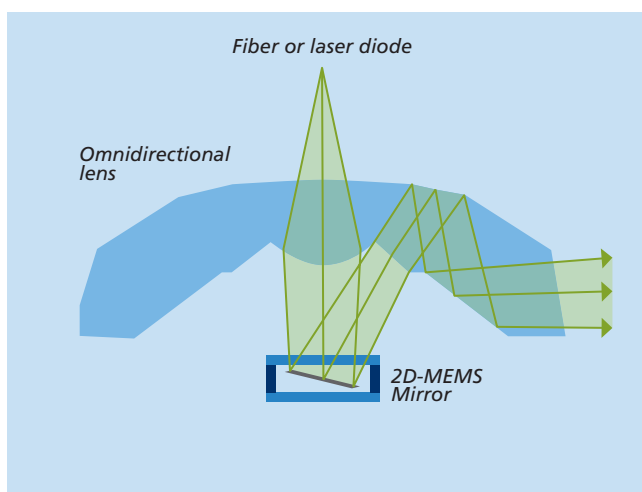
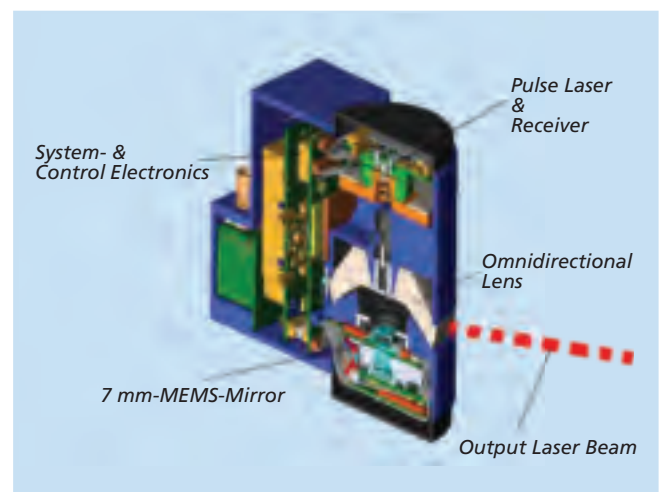


Figure 2: Cross-sectional view on the MiniFaros automotive Laser Scanner



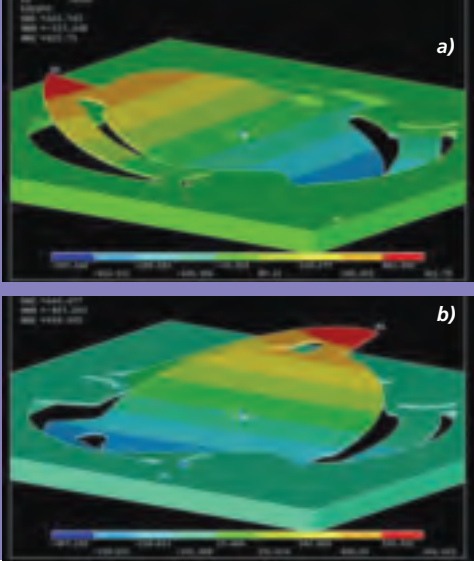


Figure 3: FE based modal analysis of the biaxial tripod MEMS mirror. Circular scanning is to be enabled by two tilting eigenmodes at $f=1.5$ kHz (first axis a) and second axis b



Figure 4: Comb drive electrodes are directly attached to the $60\ \mu\text{m}$ thick bending beams providing a very compact design

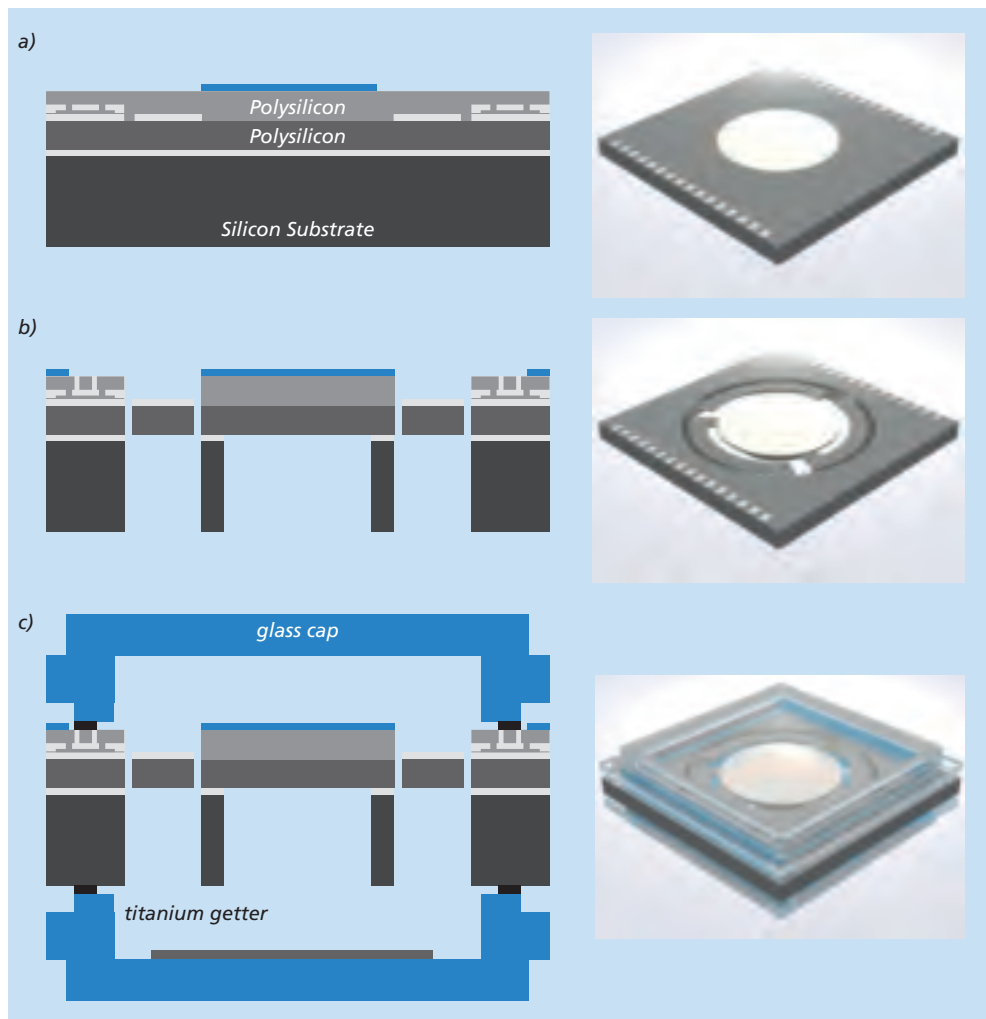


Figure 5: MEMS mirror fabrication and wafer level vacuum packaging

an omnidirectional field of view. This is achieved by combination of an omnidirectional lens and a MEMS mirror (figure 1). The divergent exit beam of a fiber coupled near-infrared pulse laser diode ($\lambda = 905$ nm) is collimated and then directed onto a large MEMS mirror, which reflects and scans the beam on a circular trajectory along the input facet of an omnidirectional lens. After passing several reflective beam-forming surfaces,

the emitted laser beam exits the optical system in horizontal direction. This arrangement allows to scan a horizontal plane within an angular range of 360 degrees. When the emitted pulse hits a target, the laser beam is partially reflected back. The backscattered pulse reenters the omnidirectional lens, passes the MEMS mirror again and enters an avalanche photodiode (figure 2).



Figure 6: Fabricated biaxial 7 mm tripod mirror for a low-cost automotive laser range sensor

The omnidirectional scanning concept requires a biaxial MEMS mirror that is capable to deflect an incoming laser beam on a circular trajectory. Since the sensor range correlates with the light collecting capability, a very large mirror aperture size of 7 mm is required. To fulfill the targeted sensor dimension of 4x 6x 6 cm³ the opto-mechanical sensor setup also requires a large mechanical mirror tilt angle of ± 15 degrees in both axes.

Target MiniFaros MEMS mirror specification

Mirror aperture size	7 mm
Scan axes	2
Scan trajectory	Circle
Mechanical tilt angle	± 15 deg
Mirror flatness tolerance	$\leq \lambda/2$

A circular trajectory requires two orthogonal axes of identical scan frequency. For that purpose, a tripod MEMS mirror design has been chosen. To consider automotive requirements with regard to shock and vibration sensitivity, a scan frequency of > 1 kHz was targeted. The curved bending beams of the tripod mirror have a length of 6.5 mm, a width of 1 mm and a thickness of 60 μm . In order to fabricate a 7 mm MEMS mirror that exhibits low static and dynamic deformation, it is necessary to realize a mirror of at least 500 μm thickness. The tripod MEMS mirror shows two orthogonal tilting eigenmodes at 1.5 kHz enabling the circular scanning (figure 3).

The biaxial 7 mm MEMS mirror is actuated by electrostatic comb drives. Wafer level vacuum encapsulation effectively reduces viscous damping and thereby enables to achieve

large oscillation amplitudes of the resonant MEMS mirror. Besides energy conservation by reduction of damping, a hermetic package effectively protects a MEMS device against contamination and failure by moisture or particles. The MEMS mirror design features stacked comb electrodes that are placed in radial orientation at the outer edge of the three identical bending beams as shown in figure 4. Several hundred finger electrodes are directly attached to the curved bending beams, building three individually addressable comb drives and three sensor combs for capacitive feedback, each comb rotationally separated from the next by 120 degrees.

The MiniFaros MEMS scanning mirrors are being fabricated on n-doped 8-inch silicon substrates of 725 μm thickness (figure 5). One of the key-features in the fabrication process is the deposition of thick polysilicon SOI-device layers in an epitaxial reactor using SiH_2Cl_2 (Dichlorosilane) as a precursor. Two 30 μm thick polysilicon device layers are produced on top of a thermally oxidized silicon substrate. Each deposition step is followed by chemical mechanical polishing (CMP). Embedded between these two polysilicon device layers, there is a double TEOS oxide layer that, on one hand, serves as a buried oxide etch-mask and on the other hand is needed to electrically isolate a thin polysilicon interconnection layer that is embedded in between these two layers of TEOS. Patterning of this interconnection layer is performed before deposition of the second TEOS layer. The buried oxide hard mask is patterned before deposition of the second polysilicon device layer by applying photolithography and dry-etching. After deposition and CMP of the second polysilicon device layer, a titanium-silver stack is sputtered on top and wet-chemically patterned to serve as high reflective mirror coating. The front side structuring is finished by a DRIE etching process that defines the upper and lower comb electrodes, mirror and the tripod bending beams. This patterning step uses a combination of a photoresist mask and the already described

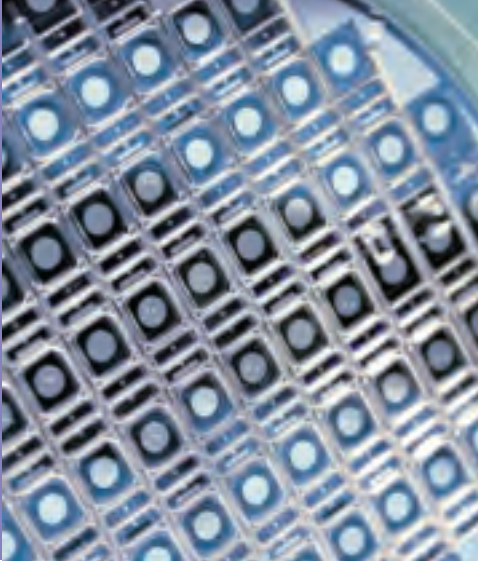


Figure 7: Biaxial tripod MEMS mirrors vacuum packaged on wafer level

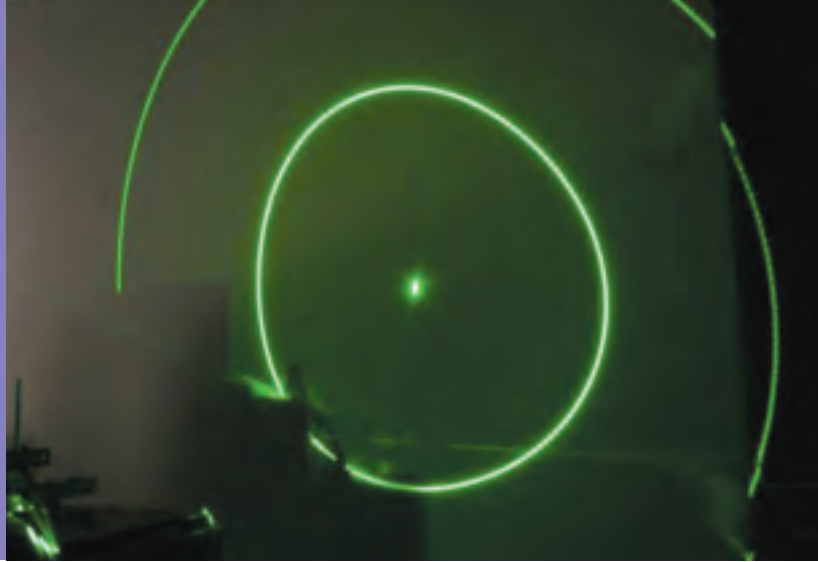


Figure 9: Circular trajectory scanned by 7 mm tripod mirror with a repetition rate of 1.5 kHz. The second circle refers to laser light that passes the mirror twice because of partial reflection at the glass lid. The center spot is also caused by direct laser reflection at the glass lid

buried oxide hard mask. In a second DRIE step, the reverse side of the MEMS mirror actuator is structured. HF vapor phase etching is applied for final release of the MEMS mirror. The fabricated tripod 7 mm MEMS mirror is depicted in figure 6.

The wafer level packaging process applies glass frit bonding of the front side and back side cap wafers to the MiniFaros MEMS wafer at temperatures above 400°C. Activation of a titanium thin film getter effectively reduces the pressure inside the cavity and minimizes damping.

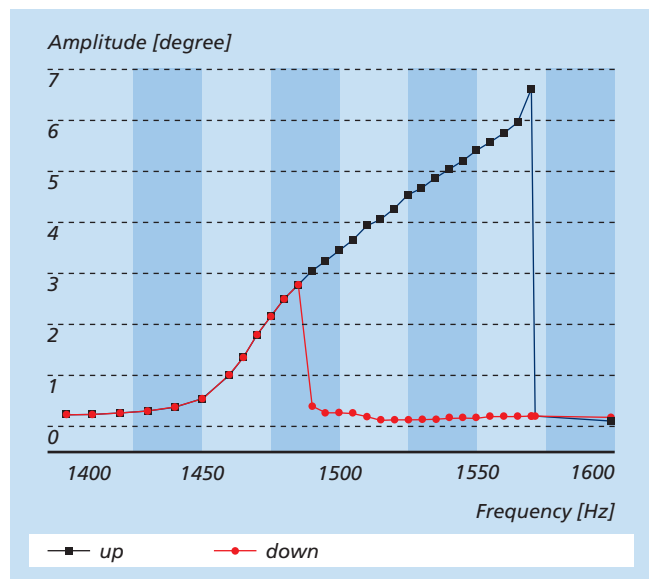
The MiniFaros tripod mirrors have been designed in different versions with regard to spring stiffness and stiffening structures and therefore show circle scanning capability with scan frequencies ranging from 500 Hz to 1.5 kHz.

The MiniFaros MEMS mirrors so far have shown Q-factors of 10,000. The mirror first starts to oscillate in one axis only, but by increasing the drive frequency the amplitude increases and more and more energy gets coupled into the second axis until a circular trajectory is achieved (Figure 9). The typical nonlinear frequency response curve is shown in figure 10.

Figure 8: Vacuum packaged MiniFaros MEMS mirror chips. The left picture shows a device where a reflow glass cap wafer has been used. The right picture shows an alternative wafer level package based on a stack of seven wafers



Figure 10: Frequency response of the MiniFaros MEMS mirror for upward frequency sweep and downward frequency sweep



HARVESTING ENERGY FROM HEAT: THE SIEGEN PROJECT

Micro-harvesters can collect tiny amounts of energy from light, heat, movement or pressure, and transform them into electrical currents - just enough to operate one of today's ultra low power microcontrollers that will provide smart functionality to a completely wireless system. Although the primary impact on our CO₂ footprint is negligible, benefits like saving millions of batteries per year motivate extensive research on energy-autonomous sensing and control solutions. The project SIEGEN targets harvesting of thermal energy in high-temperature environments.

Commercially available small thermo-generators mostly use materials that are not compatible with requirements for large volume production. As an example, the project coordinator Micropelt GmbH (www.micropelt.com/tech/technology.php) already manufactures thermo-electric generators based on Bismuth Telluride (Bi₂Te₃). Despite its physically much less pronounced thermoelectric effect, Silicon Germanium (SiGe) is also a suitable material system, with the huge advantage of an excellent technology base due to its compliance with silicon technology. This can be seen as an enabling factor for mass production that will drive down the costs of such harvester elements.

The goal of the project SIEGEN (Silicon based high temperature thermo generator on 8"-Wafer-Level) is to develop a silicon-based manufacturing process at Fraunhofer ISIT that can easily be transferred to other locations, like older CMOS lines. These energy harvesters will target environments with temperatures as high as 600°C. Application contexts could be the following:

- Autonomous sensors in industrial environments, aeronautics or automotive: Energy harvesting facilitates the installation of smart sensor systems, stretches maintenance cycles e.g. for battery replacement, and reduces the weight of a car or airplane by avoiding cables.

- Extended functionality like in-situ monitoring in gas stoves: The electrical access with cables is difficult, while self-sustained wireless systems can easily be brought into and removed from hermetically closed chambers.

Active layers in a thermoelectric harvester

The functional principle of a thermo-electrical device is based on the Seebeck effect: Like it is known from thermocouple sensors, the output voltage is proportional to the temperature gradient between a hot side and a cold side. The physical effect is based on two materials with different Seebeck coefficients. On Silicon based thermoelectric material, this can be achieved by changing the doping type: n-doped Silicon contains a small amount of Phosphorus, while p-type doping involves Boron implantation. The n-doped layers have a negative Seebeck coefficient, the p-doped layers a positive one.

However, the Seebeck coefficient is not the only figure of merit for a thermo-electric harvester: A thermal "short-circuit" across the thin junction layer would immediately reduce the temperature gradient to zero and annihilate the electrical potential. For a good performance, the thermal insulation is tailored by two basic measures: First, the Silicon is mixed with Germanium, a semiconductor with a very good material compatibility to Silicon. As reported in literature (Dissertation Martin Wagner "Simulation of Thermoelectric Devices", Technische Universität Wien, November 2007, Kap. 4.3 (www.iue.tuwien.ac.at/phd/mwagner/node51.html), adding a certain Germanium content reduces the thermal conductivity. Second, a layer thickness of about 50 µm is deposited to thermally separate the hot side from the cold side of the element.

The deposition of such thick layers is one of the challenges in the process development. SiGe layers are formed by Chemical Vapor-Phase deposition (CVD) equipment that is regularly used

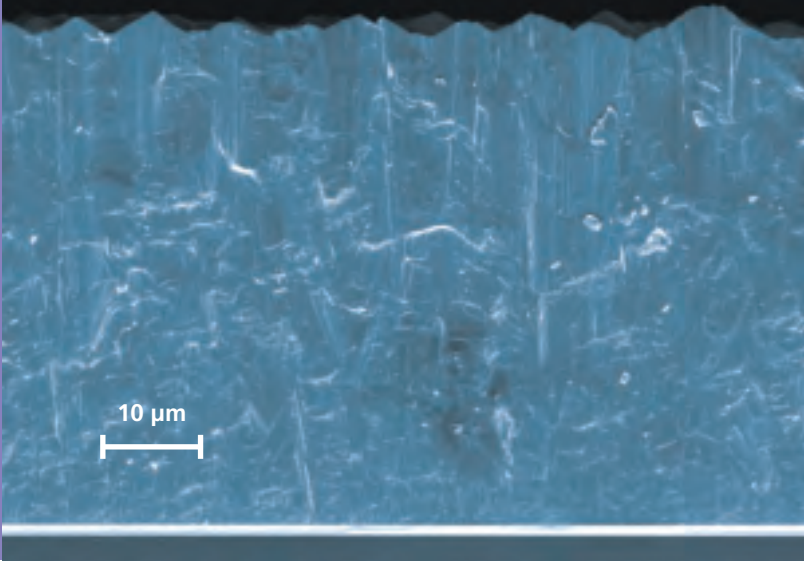


Figure 1: Cross section SEM image of an unpolished Silicon Germanium layer with a thickness of around 50 μm

for epitaxial processes. But thick polycrystalline SiGe causes strain in the multi-material layer system, and wafers experience deformation like bow or warpage. Stress engineering is therefore required to keep the wafer in a flat shape. Currently, deposition rates of 0.4 μm / min for n-doped poly SiGe and 0.2 μm / min for p-doped poly SiGe were achieved, with wafer bows below 150 μm (which is the limit for wafer processing).

Wafer Processing

What appears as the final device wafer is in fact a pair of wafers: One wafer with an n-doped functional layer and another wafer with the corresponding p-doped elements. The p-n junctions are obtained by wafer bonding, a common process in MEMS manufacturing.

Project Partners

The project consortium includes potential industrial manufacturers and users of thermo-electric energy harvester systems, as well as researchers from Fraunhofer ISIT/IPM and the University of Kiel:

- Micropelt GmbH, the project coordinator
- ABB AG Forschungszentrum Deutschland
- EADS Deutschland GmbH
- E.G.O. Elektro-Gerätebau GmbH
- Fraunhofer-Institut für Siliziumtechnologie
- Fraunhofer-Institut für Physikalische Messtechnik
- Christian-Albrechts-Universität zu Kiel
- X-FAB MEMS Foundry Itzehoe GmbH

The project is funded by the German Ministry for Education and Research.

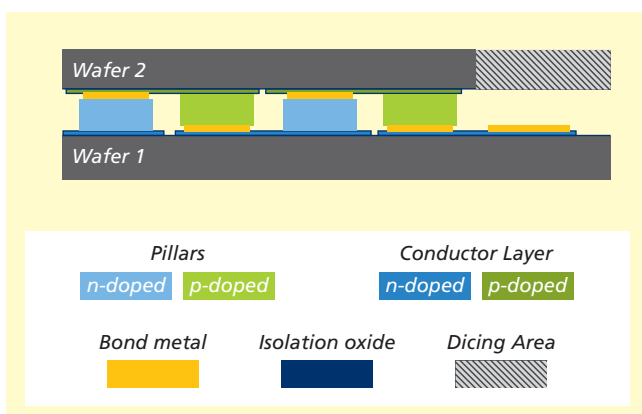


Figure 2: Cross-section (schematic) of the thermo electrical generator

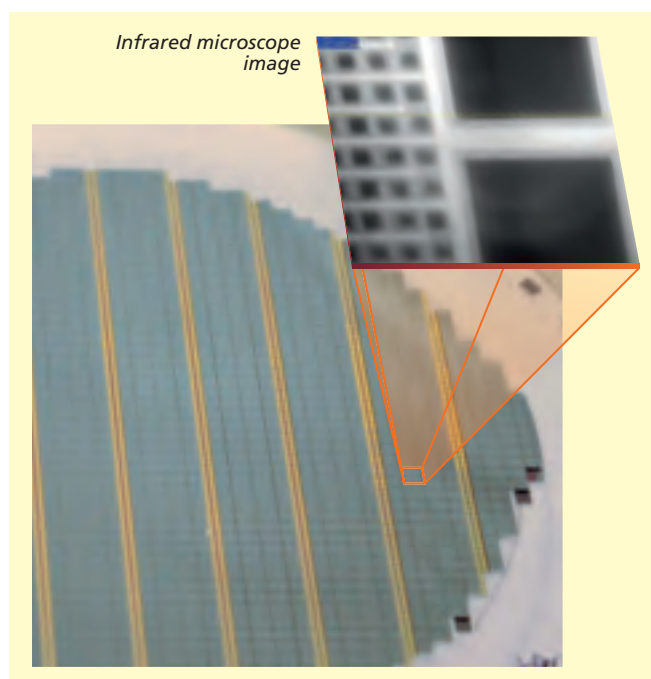


Figure 3: Wafer stack after dicing



Figure 1a: Completed construction of the engineered PZT substrate heater



Figure 1b: View of the bare wafer holder. The halogen lamps heat the wafer

THICK SPUTTERED PZT LAYERS FOR ULTRASONIC TRANSDUCERS

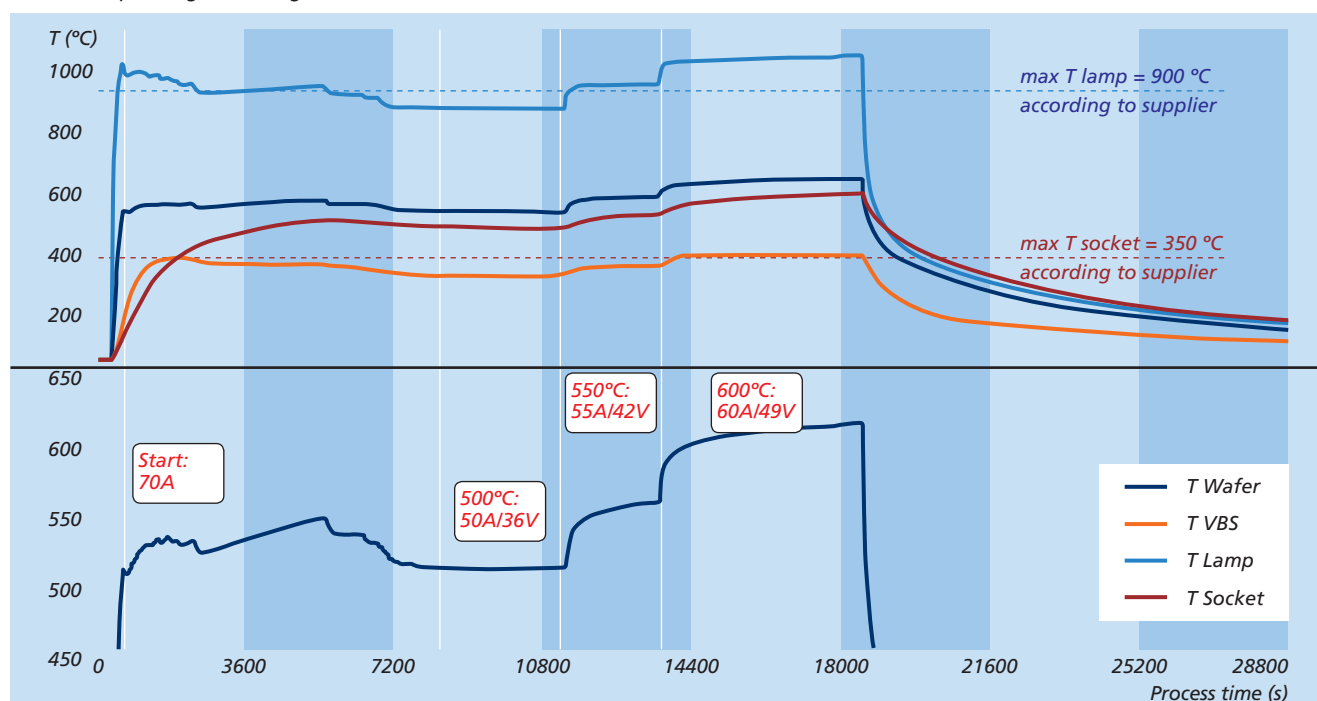
Introduction

Ultrasonic transducers play a very important role as one of the most cost effective and accurate medical imaging technologies. However, many applications demand for better resolution, which is inevitably correlated with higher ultrasound frequencies. Unfortunately, ultrasonic transducers operating at frequencies between 50 MHz and 100 MHz require geometrical dimensions far beyond the present state of the art. In the project KOLUMBUS, a new approach for the construction of high frequency ultrasonic transducers is developed. Key element is the deposition of thick high-quality

piezoelectric Lead Zirconate Titanate (PZT) layers with a minimum thickness of 20 μm . During the first year of the project, the KOLUMBUS consortium (Fraunhofer IBMT, ISIT and IST) achieved this very ambitious aim.

Starting point of the present project was the observation that highly efficient columnar Lead Zirconate Titanate (PZT) can be produced by hollow cathode sputtering or gas flow sputtering. Due to their excellent electrical and mechanical properties, the columnar PZT layers revealed to be extremely interesting for

Figure 2: Measurement of the temperatures within the wafer holder on the 8" wafer. Depending on the introduced power, temperatures rise to over 600°C on the silicon wafer. For the deposition of the PZT layers, however, typically temperatures in the lower 500°C range are used, corresponding to heating currents of about 50 A



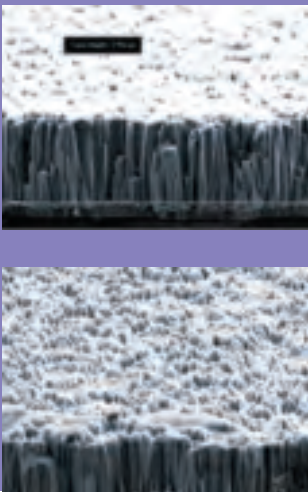


Figure 3: SEM image of a 3 μm thick PZT film. The columnar structure is clearly visible

the design of high-frequency ultrasound transducer systems. The gas flow sputtering process developed by Fraunhofer IST allows the generation of thick PZT layers on full-sized 200 mm (8") wafers at relatively low process temperature (500°C to 600°C), with a high sputtering rate of 100 nm/min. While the previously reached thickness on 150 mm (6") silicon wafers was already slightly above 10 μm , a layer of 25 μm thickness could be achieved in this work. Moreover, the distinctive columnar structure of the sputtered PZT layer together with its intrinsically low film stress allows the crack-free preparation of such thick PZT films on silicon.

Construction of a Halogen Lamp Heated High Temperature 8" Wafer Holder (IST)

In the first year, the new construction of the 8" high-temperature wafer holder was completed. The specific construction became necessary when the entire process technology of ISIT was switched to 8" wafer format. The previously used wafer

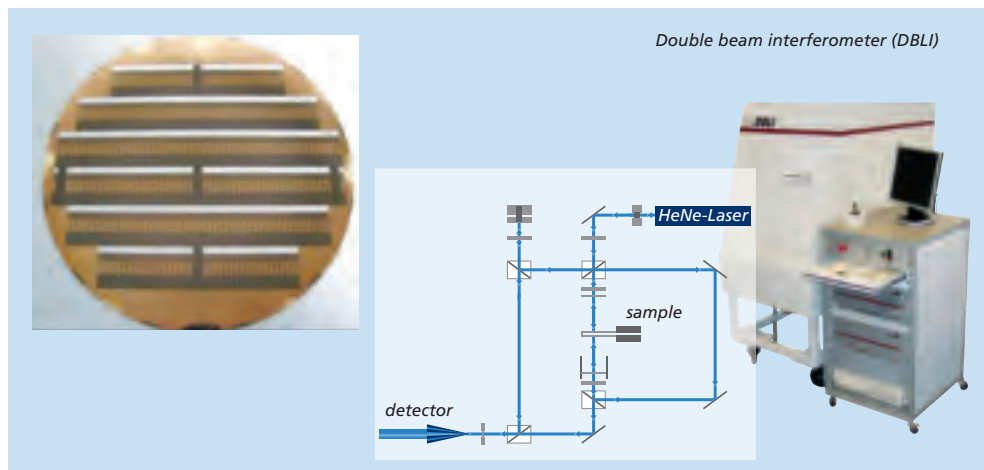
holder was too small and too weak for handling wafers above 6" in size. The newly built 8" tool uses special halogen lamps arranged in a ring around the heated wafer. After a few test cycles, it could successfully be used at temperatures up to 600°C. Former coating experiments applied substrate temperatures ranging from 520°C - 550°C to achieve good results.

Material Development and Characterization (ISIT, IST)

One of the main objectives in the first project period was the development of the gas flow sputtering process for thick PZT layers on 8" silicon wafers. In order to ensure an optimal growth of the PZT in the required perovskite phase, all wafers were previously provided with a layer of platinum, which in the later production processes is used as bottom electrode. For the characterization of sputtering quality, test wafers at various process parameters were coated with a 2.5–3.5 micron thick PZT layer. For judging the quality of PZT layers, the piezoelectric coefficients are generally the most important parameters.

Figure 4 left: Structured 200 mm wafer for piezoelectric and electrical characterization of PZT films

right: DBLI measuring principle and setup for piezoelectric characterization. The total thickness of the wafer is measured by interferometry. A falsification of the results by piezoelectrically induced bending of the wafer can be avoided in this way



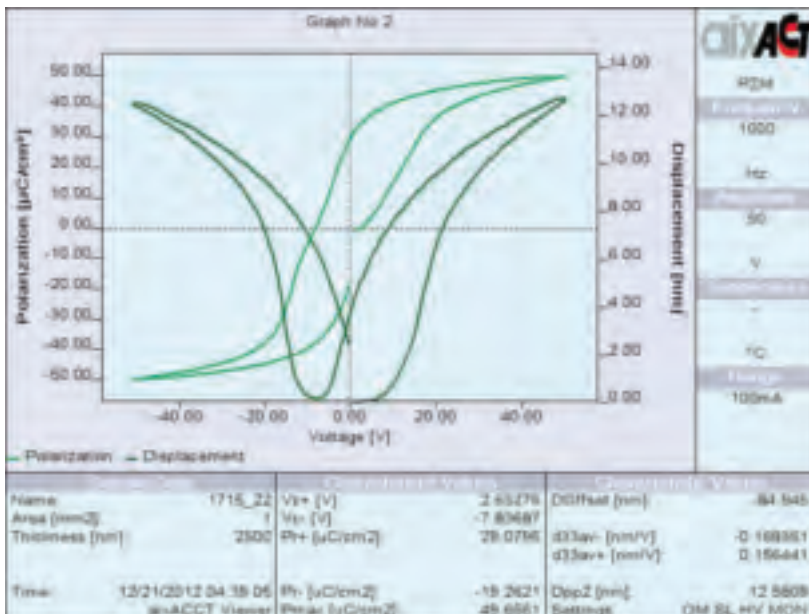


Figure 5: Measuring the coefficient $d_{33,f}$ of a 2.5 micron thick PZT layer by double beam laser interferometry (DBLI). The mean values $d_{33,f}$ moved to 160 pm/V, a very good value for PZT thin films

On the patterned PZT layer, the top electrode is provided by a gold structure (figure 4a). Subsequently the wafers are examined and, beside the determination of their electrical characteristics, the piezoelectric coefficient of the PZT layer $d_{33,f}$ is measured. For this purpose, the double beam laser interferometry (DBLI) (figure 4b) is used, which allows the reliable measurement of the pure vertical elongation of the PZT layers in dependence of the applied electric voltage. During the development process, first PZT films were prepared with 2.5 µm thickness. Heating with a current of 50 A during the sputter process was sufficient to deposit thin films with very good piezoelectric coefficients (figure 5). The films showed a pronounced columnar structure of the PZT without exception.

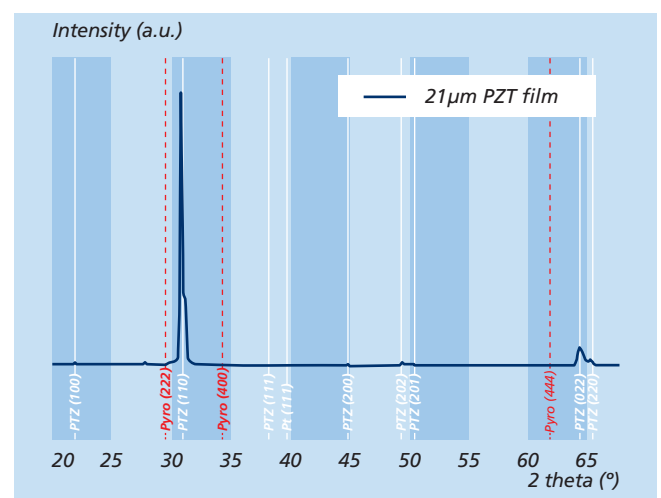
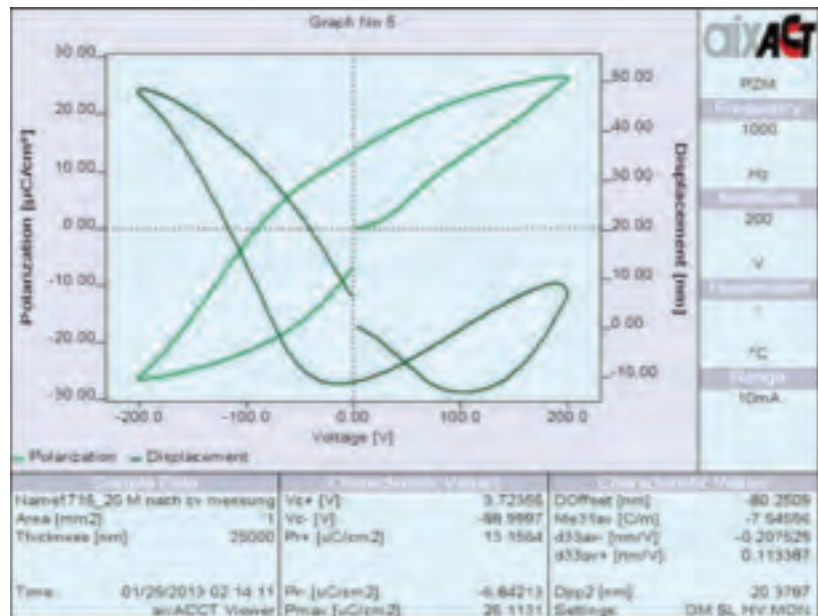


Figure 7: The X-ray crystallographic analysis confirms the quality of the thick PZT layer. In this 2-theta diagram, only peaks corresponding to a pure perovskite phase of PZT can be identified



Figure 6, above: 21 micron thick, gas-flow sputtered PZT layer in a cross section. During the sputter process, the wafer holder was heated with a current of 50 A
bottom: The same layer as in Figure 6a, this time at a steeper angle. The rough surface of the layer can be seen clearly

Figure 8: Piezoelectric characterization of a 25 micron thick layer of gas-flow sputtered PZT in a large-signal measurement



Deposition of Thick PZT Layers (IST, ISIT)

In the second development step, the deposition of thick PZT films was studied and optimized. Different sputtering parameters and their effect on the PZT structure and quality were considered. Crack and void free layers of up to 25 microns were successfully deposited on platinum-coated silicon wafers. The distinct columnar structure of the layers is clearly visible in the SEM images (figure 6a, b).

Both the X-ray crystallographic analysis and the piezoelectric characterization provided excellent results. The films exhibited no non-perovskite phases according to the XRD diagrams (figure 7), and $d_{33,f}$ coefficient values were found between 200 pm/V and 250 pm/V (figure 8). In summary, it can be stated that the planned objectives for the first project phase have been achieved completely. The required layer thickness as well as the quality of the PZT meet the requirements for a

further integration into a fabrication process for an ultrasound transducer. Based on this thick PZT layer, an ultrasonic transducer for 80 MHz ultrasound is under development.

BMBF Projekt – VIP Programm

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Projektpartner:
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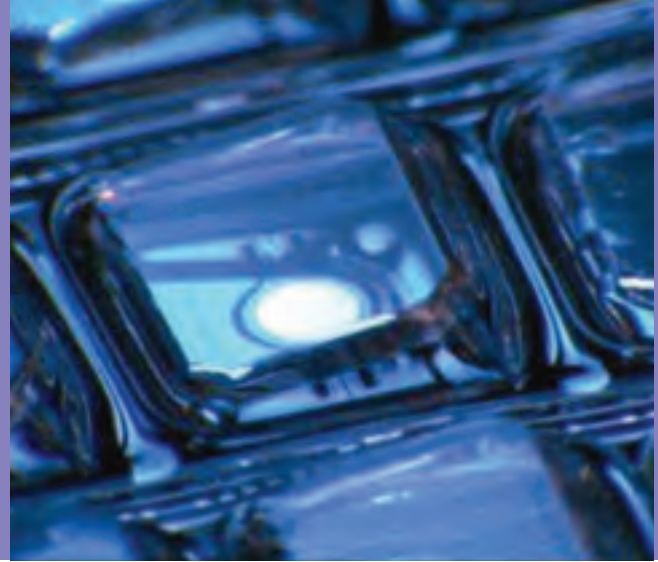


Figure 1: Close up of a wafer level vacuum packaged mirror with an inclined window (window size: 3.3x 4.5 mm)

DEVELOPMENT OF A NEW TECHNOLOGY FOR GLASS PACKAGES WITH INCLINED OPTICAL WINDOWS FOR MICRO MIRRORS ON WAFER LEVEL

Introduction

Hermetic wafer level packaging of MEMS under vacuum is well established for products like gyroscopes or multi-axis accelerometers, which are inconceivable without such encapsulation techniques. In contrast, solutions for micro-optical devices with integrated actuators (MOEMS) typically still use non-vacuum or device-level packaging, thus suffering from elevated costs and sometimes reduced performance.

The application of suitable glasses as cover lid for MOEMS device integration on wafer level ensures high optical transparency and hermetic sealing of the device simultaneously. Hermetic glass packaging is a very attractive solution for many applications, offering long term stability and protection against particles or humidity immediately after processing the microstructures in the cleanroom.

Micro mirror devices are among the MEMS devices that are increasingly gaining interest for consumer products, like embedded pico projectors in smart phones and digital cameras, and in automotive applications, e.g. head up displays. The packaging of these devices more and more enters into the focus of research. High-vacuum packaging technology has a tremendous impact on the performance of micro mirrors, because it allows to build faster, larger mirror plates that enable sharp, bright and flicker-free HD projection across long distance.

The Fraunhofer ISIT has been dealing with the development of micro mirrors for many years. A unique technology for the production of glass packages now greatly reduces the costs of these devices: Inclined optical windows are manufactured from 200 mm glass wafers, which consequently can be used as optical cap elements in a full wafer bonding process.

Motivation

The micro mirrors developed by Fraunhofer ISIT are designed to achieve large optical scan angles at moderate driving voltages, which can only be realized under vacuum. Because conventional solutions for discrete vacuum packaging are too expensive for mass production, a wafer level vacuum encapsulation is an attractive goal. However, scanning micro mirror devices require a sharply defined laser beam to avoid imaging artifacts. The laser generally is located outside the MEMS package, which means that it passes the optical window twice, on entry and on exit. Although glass wafers with high optical quality are available, there is another major issue: Usually, the basic orientation between the glass cover and the micro mirror is more or less parallel, thus a bright laser spot appears in the projected image due to partial reflections of the incident intense laser beam on the cover glass surface. An anti-reflective coating (ARC) on the transparent surfaces only reduces the intensity of the observed central reflection to a minor extent: Since the incoming laser beam delivers the complete light for the projection image, any optical reflection must be reduced to an extremely small fraction (less than 10^{-7}) of the incident laser intensity, which is far beyond the performance of any available ARC.

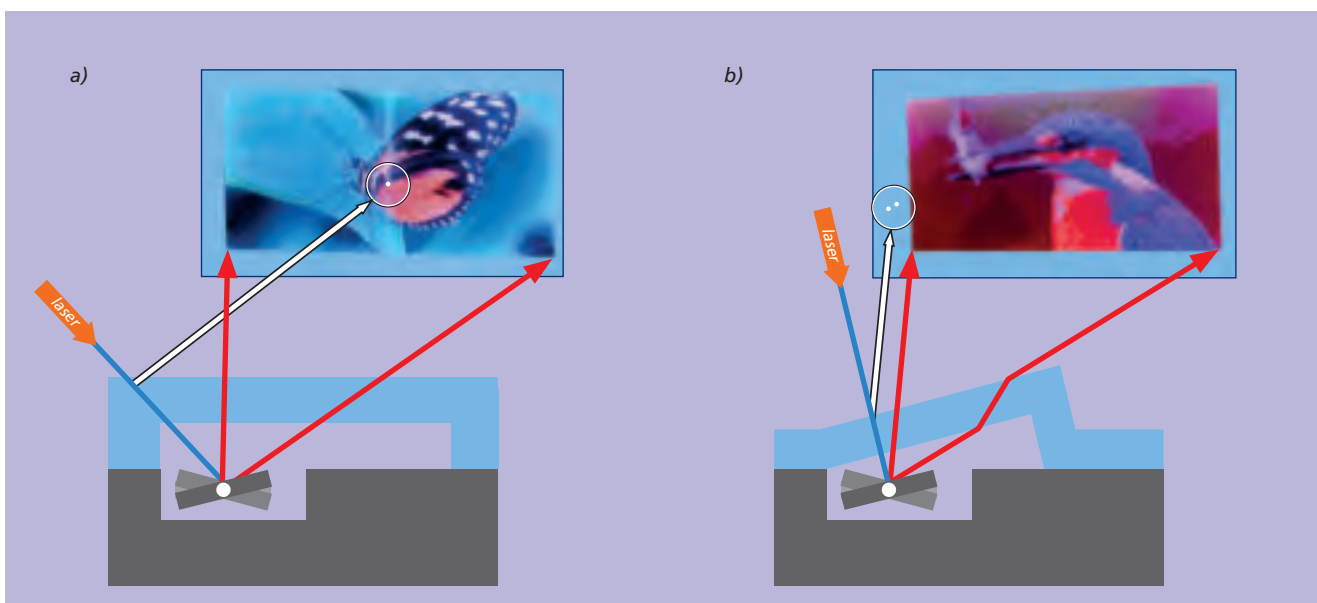
A complete elimination of the central reflection in the image can only be achieved by geometrical means, i.e. by using an inclined optical window that deviates the undesired outer reflection part of the incident beam to a place outside the projection field. However, inclined high quality glass surfaces on complete wafers with dimensions in the mm range cannot be

produced using standard micro machining, while conventional hot forming glass fabrication techniques like precision molding are limited in the size of the glass substrate (< 70 mm) and their surface qualities. Therefore, a new process has been developed for the fabrication of a plurality of inclined optical surfaces on a 200 mm wafer.

Technology

The process for the fabrication of the glass packages with inclined surface is based on high-temperature viscous glass micromachining. A sequence of anodic bonding steps of silicon wafers to a borosilicate glass wafer is applied, involving 200 mm wafers (725 μm thick silicon and 725 μm thick borosilicate glass) according to SEMI standard specifications.

Figure 2: Schematic of the wafer level packaging concept: (a) Flat cover: The reflex results in a bright laser spot in the image. (b) Inclined cover: The window is inclined by roughly 15°. The mirror amplitude is +/- 15°, so the reflection is outside of the image area and can be blocked by an aperture



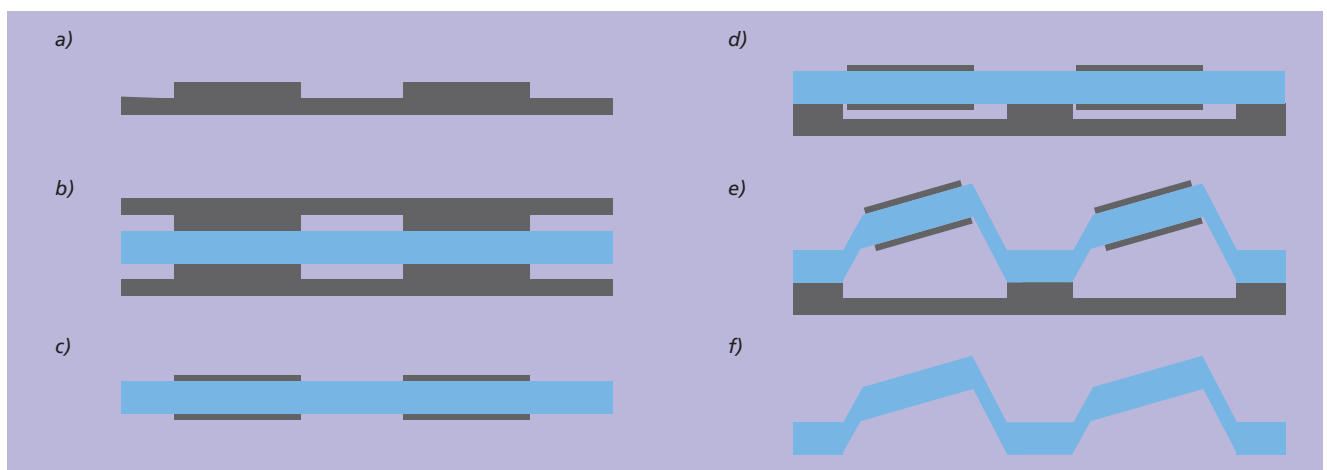


Figure 3: Schematic of the process flow for the glass wafer. While the window area moves outward, a surrounding socket is formed around the reinforced element: This socket creates additional volume for the free movement of the encapsulated micro mirror, which makes an additional spacer wafer obsolete

First, deep cavities are etched into two silicon wafers with a DRIE process step (figure 3a). These two structured silicon wafers are anodically bonded on both sides of a borosilicate glass wafer (figure 3b). For this step, it is necessary that all wafers are very clean and particle free. A double-side wafer grinding step isolates the glass-silicon contact areas into a pattern of silicon islands (figure 3c). The grinding process introduces residual stress in the silicon, hence it is essential to perform a short stress relief step in order to avoid a resulting warpage in the optical window areas. The glass wafer with its silicon island structures on both sides is then bonded to a third silicon wafer, which provides pre-defined cavities enclosing the silicon islands (figure 3d). During the last anodic bonding step, a nitrogen atmosphere is enclosed in the cavities with pre-adjusted pressure of about 950 mbar. The composite wafer is then annealed above the softening point of the glass material (figure 3e). Due to the thermally enhanced pressure difference between the cavities and the oven atmosphere above 680°C, the stacked silicon-glass elements inside the cavities

slowly move outwards. As a consequence of the asymmetric arrangement of silicon islands in the cavity, an inclination of the silicon-glass elements can be observed. Finally, a KOH wet etch step selectively removes all the silicon from the glass wafer (figure 3f). The exposure of the glass surface to the KOH must not exceed a certain limit, to avoid generation of defects and roughness on the window areas. The bonding of the processed glass window wafer to the micromechanical mirror wafer is done by glass frit bonding.

Glass Package with Inclined Surfaces

The surface quality of first glass packages has been investigated using a white light interferometer. The measurement was done on the outer surface of the glass cap, on a single die level. The smaller side of the glass package has approx. 100 nm, the longer side approx. 300 nm curvature. This is well below the estimated required flatness for the glass cap.

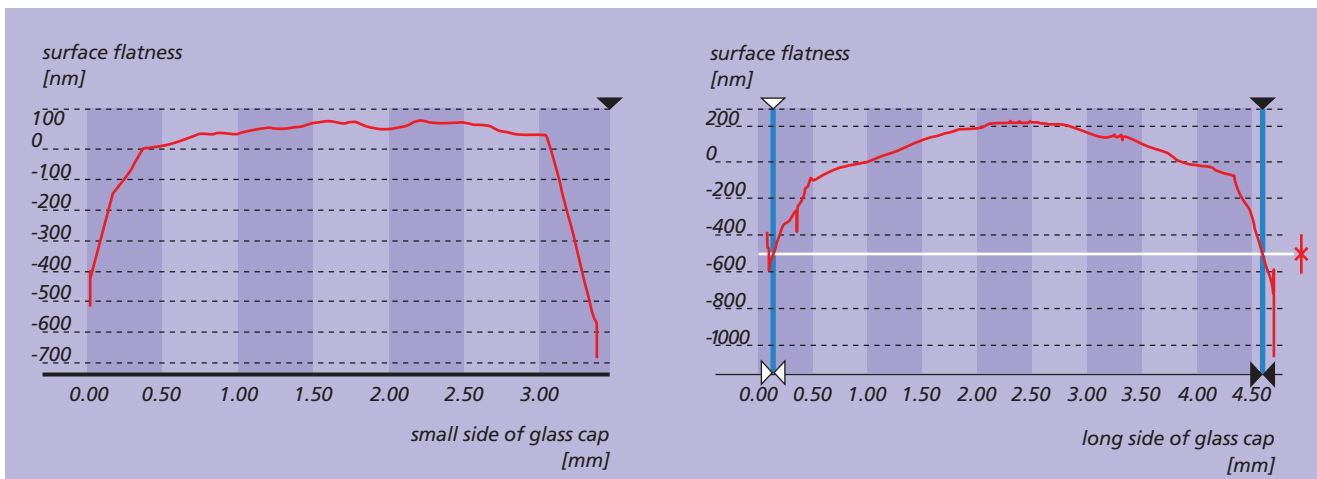


Figure 4: White light interferometer measurement of the window surface to determine flatness of a single glass package. Left: Measurement along the small side. Right: Measurement along the long side

Conclusion and Outlook

The first processed glass wafers with inclined optical windows demonstrate the capabilities of the new glass forming technology. The glass caps showed an optical quality that is well suitable for packaging optical devices like ISIT's micro mirror devices.

Recently, first micro mirrors have been successfully packaged under vacuum using inclined glass caps. The characterization and test of these mirror devices with two glass package variants is still ongoing. The process improvement of the viscous glass forming technique is continued.

This work was presented at the Eurosensors Conference in Krakow in 2012 and Ms Vanessa Stenchly was honored with the best poster award in the Young Scientists category.

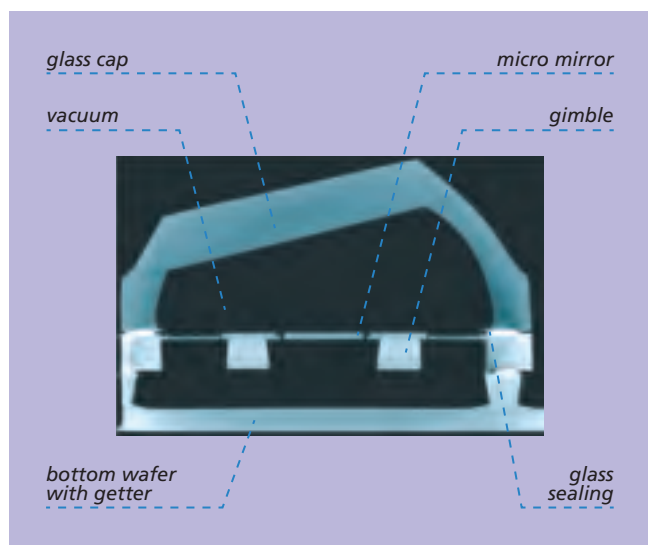


Figure 5: The X-Ray computer tomography cross section through a fully capped mirror-device shows (top to bottom) the glass cap, the micro mirror and the bottom wafer

THIN FILM PZT RESONANT SINGLE AXIAL MICROMIRROR WITH HIGH FREQUENCY AND LARGE DEFLECTION APPLYING LOW DRIVING VOLTAGE

Micromirrors are of high interest for automotive and consumer applications, because of their small dimensions, low power consumption and cost efficiency. They can enable applications such as head-up-displays, optical switches and laser projection displays. The driving technologies used for micromirrors are mainly based on electrostatic, electromagnetic, thermal and piezoelectric principles. Piezoelectric materials are suitable for actuating MEMS devices because the materials produce forces caused by the deformed crystals, when voltages are applied on them, as shown in figure 1. Reversely, voltages exist also under applied forces because of the shifted charge centers of the crystals.

Compared to other actuators, a piezoelectric driver is less affected by air damping, omits external force supplies and the response time is very short. Additionally, piezoelectric materials, especially PZT (lead-zirconate-titanate), can deliver

higher forces at low driving voltages. However, PZT is a relatively new material and rarely accessible for the MEMS production. Since years the processing technology of PZT has been well developed at Fraunhofer ISIT. Now ISIT possesses the competence to sputter and structure thin film PZT layers with excellent material quality, which are enabling technologies to develop the thin film PZT actuated micromirrors.

Since the invention of the first digital micromirror device, along with the constantly improved fabrication technologies, the applications of micromirrors are thus becoming versatile. The construction of a single axial micromirror for fulfilling large deflections and required high frequencies simultaneously is a very challenging task. For the design development of the PZT micromirror, FEM simulations and analytical modeling have been performed to identify an effective design fulfilling the above mentioned demands.

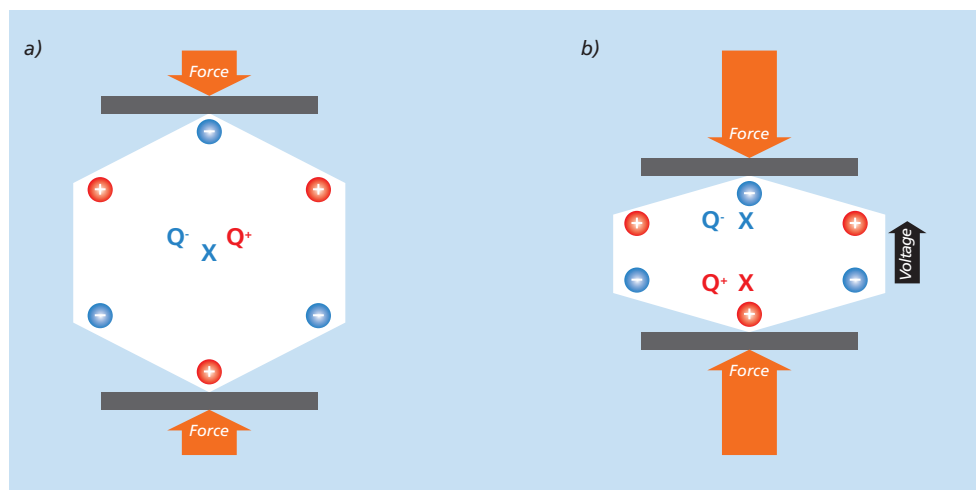


Figure 1: Piezoelectric effect: (a) Undeformed crystal of a piezoelectric material; (b) Shifted charge center of the crystal under a force causing a voltage

The presented single axial PZT micromirror is operated by two bimorph actuators, which are connected via top and bottom electrodes. The generated forces by actuators are transferred by a connecting bar from the actuators till the mirror in the center to rotate the micromirror. Figure 2 shows the cross section of a rotating micromirror and the operating actuators.

Figure 3 illustrates the design possessing a mirror in the center and an outer actuator frame, which consists of two paraphase driven, one-end-anchored bimorph actuators and connecting bars between actuators and torsion bars. The construction enables mechanical leverage amplification. Thereby, the forces from the PZT actuators are amplified and act on the micromirror, so that in the resonant torsional mode the micromirrors tilt with much larger amplitudes than the actuators ($\theta_m > \theta_a$).

Since for this work the targeted resonant frequency f and mechanical optical scan angle θ_{opt} of the micromirror are 30 kHz and 40° , $80 \mu\text{m}$ thick polysilicon substrates are used for the micromirror to gain a dynamic deformation lower than $\lambda/4$ (the used $\lambda = 635 \text{ nm}$). For simplifying the fabrication process the actuators feature the same thickness as the micromirror, which also delivers a higher mechanical stability of devices. Moreover, this thickness of actuators leads to a high frequency of the bimorph cantilevers, which enables a high resonant frequency of the complete oscillating system including actuators and micromirror.

With the identified dimensions for the presented design an effective force translating from actuator to micromirror is provided, so that the micromirror owns not only a high frequency as above mentioned but also a large scan angle.

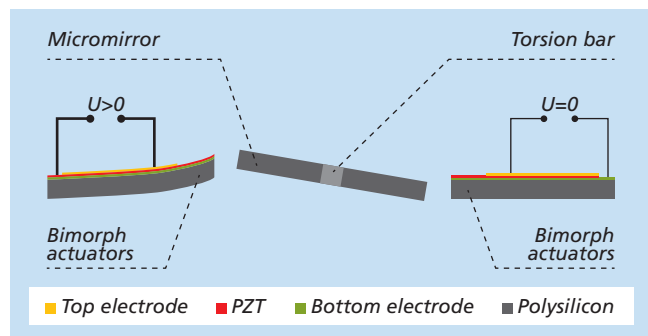


Figure 2: Cross section view of an operated micromirror driven by two PZT bimorph actuators

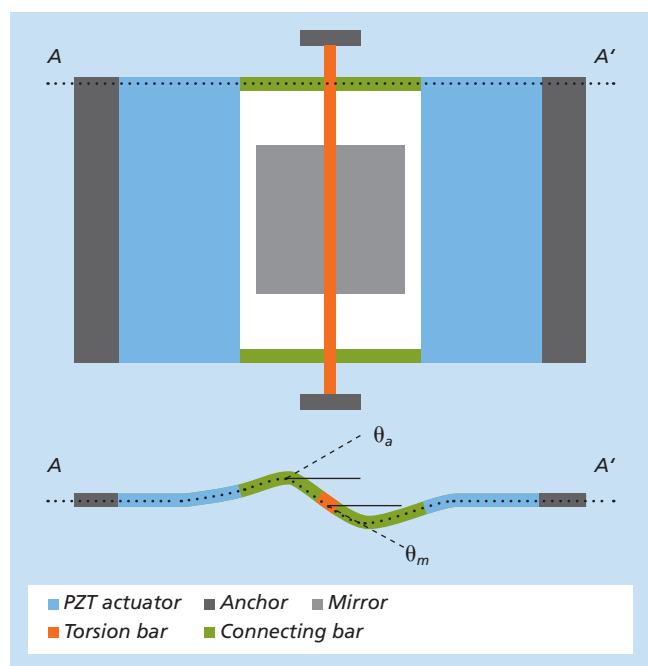


Figure 3: Top view of design schematic and cross section view of section AA' while micromirror in torsion mode with a slope θ_a in the connecting bar and a rotating angle of the micromirror θ_m

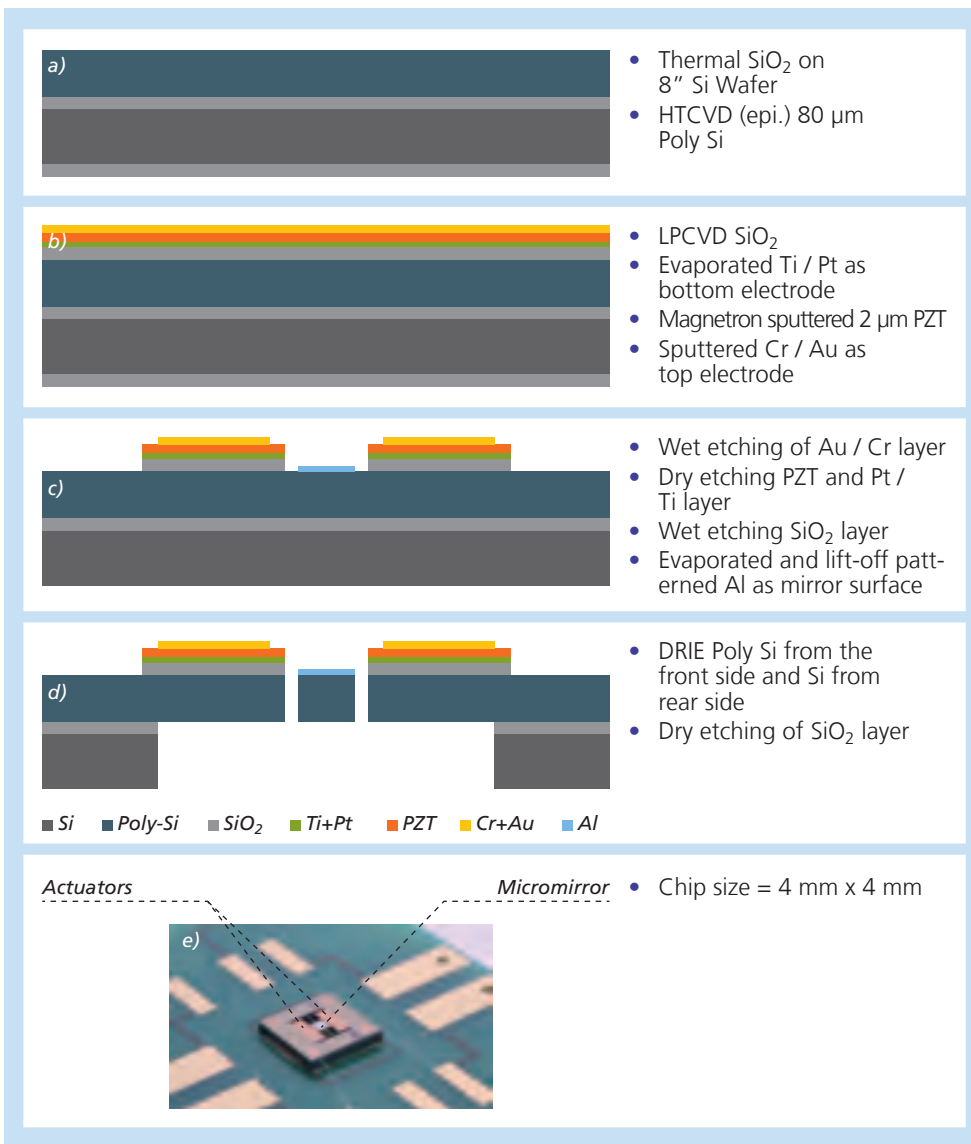


Table 1

The micromirrors are realized in a bulk silicon micromachining process, which is shown in table 1.

The characterization of fabricated devices related to the scan angle and resonant frequency of the micromirror has been performed using the measurement setup shown in Figure 4. Hereby, the beam splitter guides the laser beam onto the micromirror, while the micromirror receives a stochastic signal from the driving electronics. This stochastic signal contains a broad frequency spectrum, so that the micromirror will respond and rotate with its own resonant frequency reflecting the laser beam onto the position sensitive device (PSD), where it projects a line. The length of the projected line is proportional to the scan angle of the micromirror and is captured by the PSD, which sends a response signal back to the driving electronics. Therewith the driving electronics sends appropriate driving signals

to the micromirror, so that the micromirror keeps rotating constantly and stably. Applying this closed-loop control both the scan angle and the frequency of the micromirror are measured.

Figure 5 shows a photo of an actuated and rotating micromirror that reflected the laser beam onto a paper, resulting in a projected line. This micromirror rotated with 32 kHz in air and provided an optical scan angle of 42.5°, whereby only one PZT actuator was operated at 7 V.

Resonance curves of the fabricated devices have been recorded as well for calculating the Q-factor, which are illustrated in figure 6. The Q-factor of the resonance curve driven by 2 V lies between 1572 and 1746, while the Q-factor measured with the driving voltage of 6 V is lower and lies about 1123. For devices with such high frequencies the

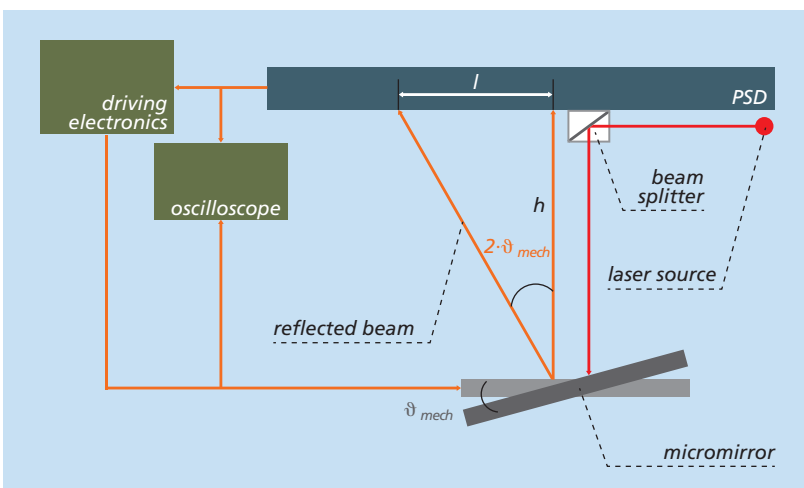


Figure 4: Measurement setup for scan angle of micromirrors

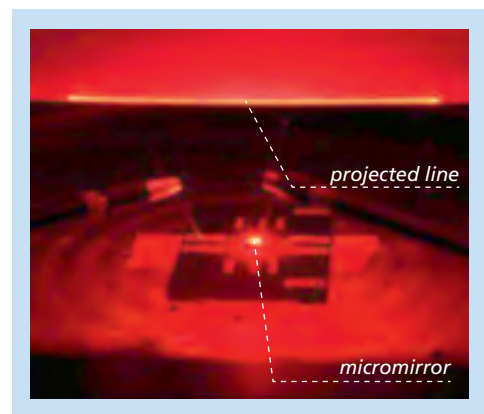


Figure 5: Projected line of a micromirror with a total optical scan angle of 42.5° and resonant frequency 32 kHz by one-actuator-driving at 7 V

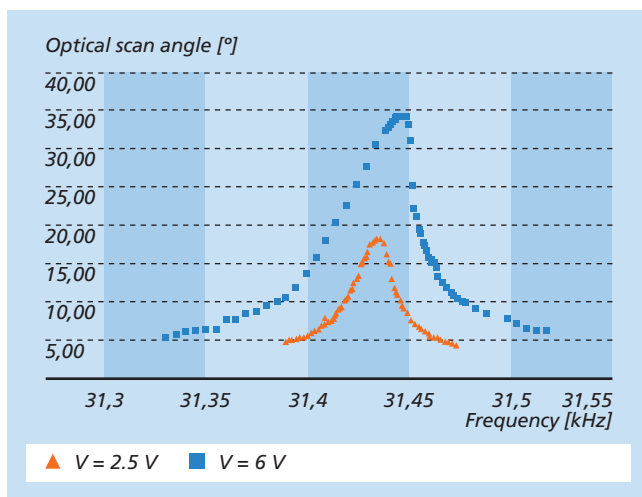


Figure 6: Measured resonance curves of a micromirror with presented design driven by one-actuator-driving with 2.5 V and 6 V, respectively

Q-factor is extraordinarily high, which indicates the low energy loss and great resonant movement of the micromirrors even driven in ambient environment.

A single axial micromirror with 1 mm² aperture has been presented featuring a large deflection, high resonant frequency and Q-factor, whereby only low driving voltages are required. Figure 7 demonstrates a comparison between several micromirrors driven by various principles, which belong to the best micromirrors presently, with the background describing the requirements for different display formats. Combining the two most important criterions for evaluating display qualities, the $\theta_{\text{opt}} \cdot D$ – Product (the product of the optical scan angle and diameter of the micromirrors) and the frequency, the presented PZT micromirror shows an outstanding performance.

Another comparison in figure 8 between the same micromirrors as above relating to the ratio of $\theta_{\text{opt}} \cdot D \cdot f$ product to driving

voltages shows that this PZT micromirror reaches a great mechanical performance and energy efficiency.

The measurement results confirm the good performance of the micromirror with regard to the high frequency and large deflection by using the leverage construction. The design flexibility is demonstrated as well, so that the suspension of the micromirror can be not only adapted for laser display purpose but also for another application by changing the geometrical dimensions. Meanwhile first measurement results indicate that the deflection angles are restricted by the stress limit of the material. Therefore, based on the presented parametric study and analysis of the results, redesigns for improving the mechanical performances, mirrors with larger apertures and other application fields are proceeded. Moreover, characterization related to long-life cycles and fatigue of the devices is also in progress.

Figure 7: Comparison of various micromirrors driven by different principles related to $\theta_{opt} \cdot D$ -product, frequency versus requirements for different display formats (A refresh rate of 60 Hz and bidirectional scanning are assumed)

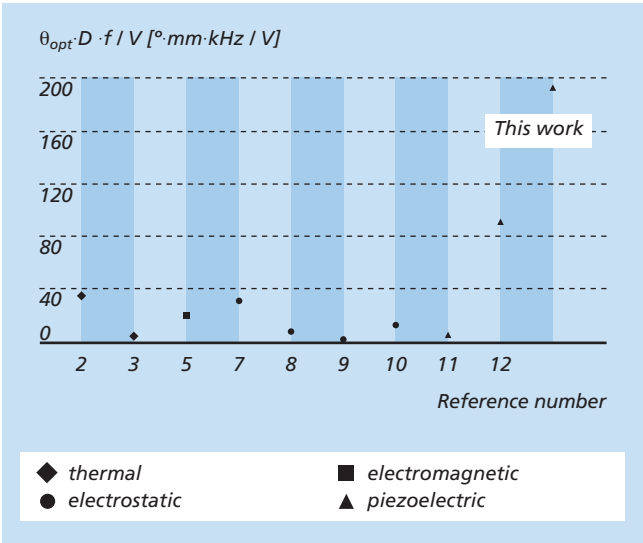
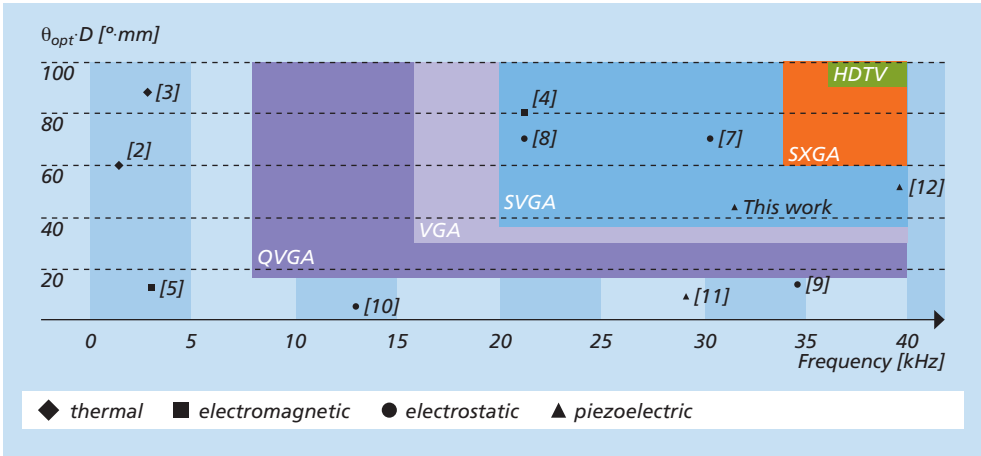


Figure 8: Comparison of various micromirrors driven by different principles related to product of $\theta_{opt} \cdot D$ -product and frequency divided by driving voltage

DEVELOPMENT OF A SMART STEPPER MOTOR DRIVER IC

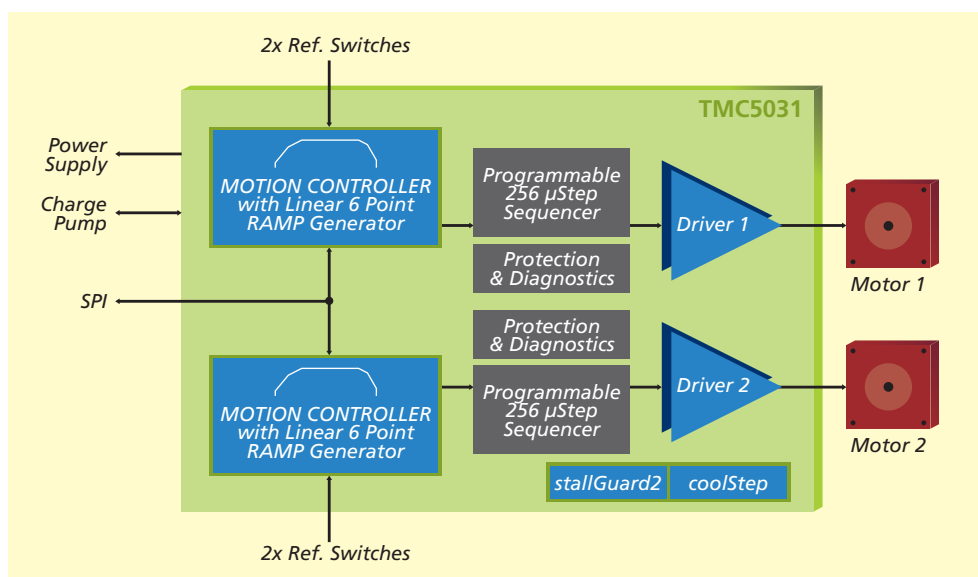
After an already long lasting collaboration, Trinamic Motion Control GmbH further intensified their cooperation with Fraunhofer ISIT. The result is the motor controller IC TMC5031, which integrates the driver and controller for two bipolar stepper motors. In addition, it includes a complex digital part with about 70,000 gates consisting of a serial interface as well as a large amount of motor specific algorithms. Furthermore, an analog part including Digital-to-Analog Converters (DAC), chopper-stabilized comparators and a band-gap reference is added; power bridges are realized with N-channel-MOSFETs to drive the stepper motors with a maximum coil current of up to 1.5 A.

What the customer sees is an intelligent interface IC that can easily be programmed and autonomously drives a motor to a given position via pre-defined velocity profiles. It dynamically

reacts on various different signals as well as motor situations. Intentionally, no programmable processor structures were used in the digital part to avoid temperature sensitive non-volatile memory and to increase the reliability by hardwired logic.

For both motors, the power part includes two full bridges driving the motor coils. Each full bridge consists of four N-channel-DMOS-FETs with 300 mΩ and 400 mΩ on-resistance, respectively. Due to the induced voltages that create a current through the body diodes of the field effect transistors, an accurate isolation between the MOSFETs themselves and the sensitive analog part was designed. The MOSFET-bridges are realized by 5V low-side gate drivers and by floating high-side gate drivers via fast level shifters. A charge-pump provides the necessary voltages above the positive supply level for the high-side drivers.

Figure 1: Functional diagram of the Trinamic TMC5031 developed in a joint collaboration with ISIT



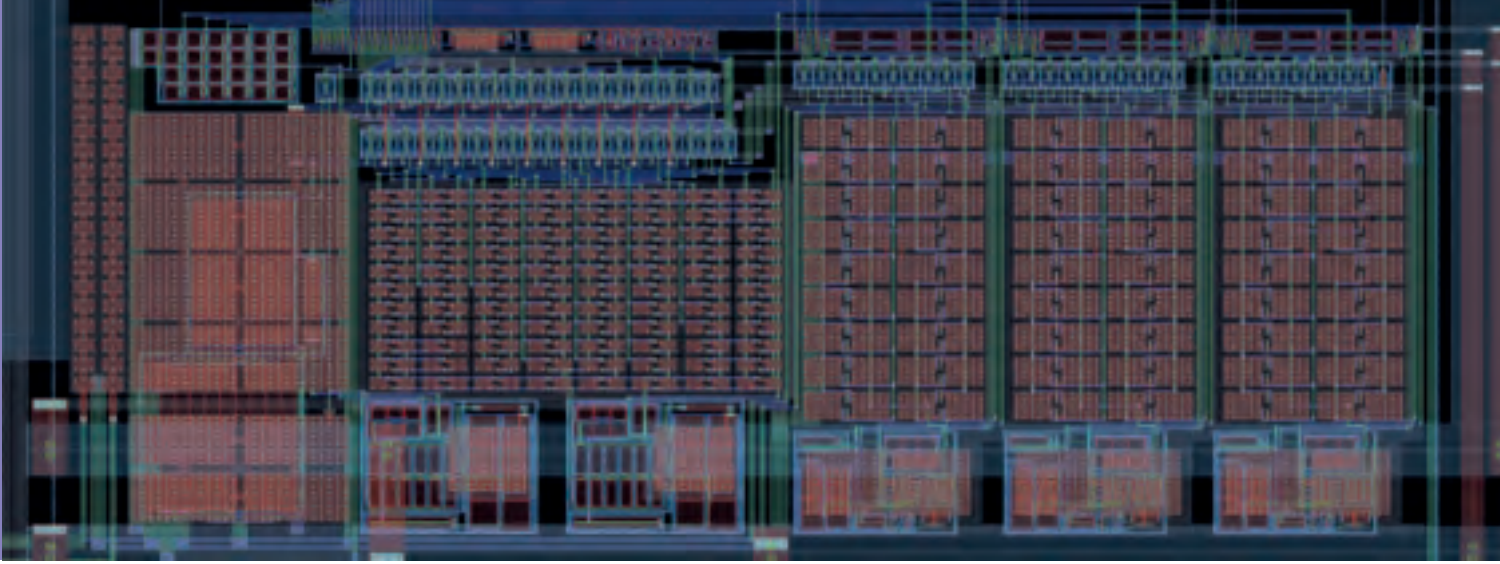


Figure 2: Partial design view of the TMC5031 stepper driver IC layout

The IC is suited for applications like CCTV cameras, heliostat-based solar power stations, printers and countless other industrial applications, including the increasing biotechnology market. These applications benefit from the integrated sensor-less features and sensor interfaces, including energy saving qualities. These attributes are included to enhance the operation reliability compared to classical stepper motor ICs, to increase the failure diagnostics and protection ability and to minimize the power consumption.

About the Dongbu 1830BD18BA – 40 V / 180 nm BCDMOS-Process

The project was implemented on a 40 V, 180 nm modular BCDMOS process from Dongbu HiTek, one of the semiconductor industry's top ten foundries in the world. The optimized power components deliver best-in-class Rsp (specific on-resistance) performance in the 20 V - 40 V space. The process provides up to 40 V NLD MOS power devices, a full suite of analog components, dense 1,8 V and 5 V logic and embedded non-volatile memory.

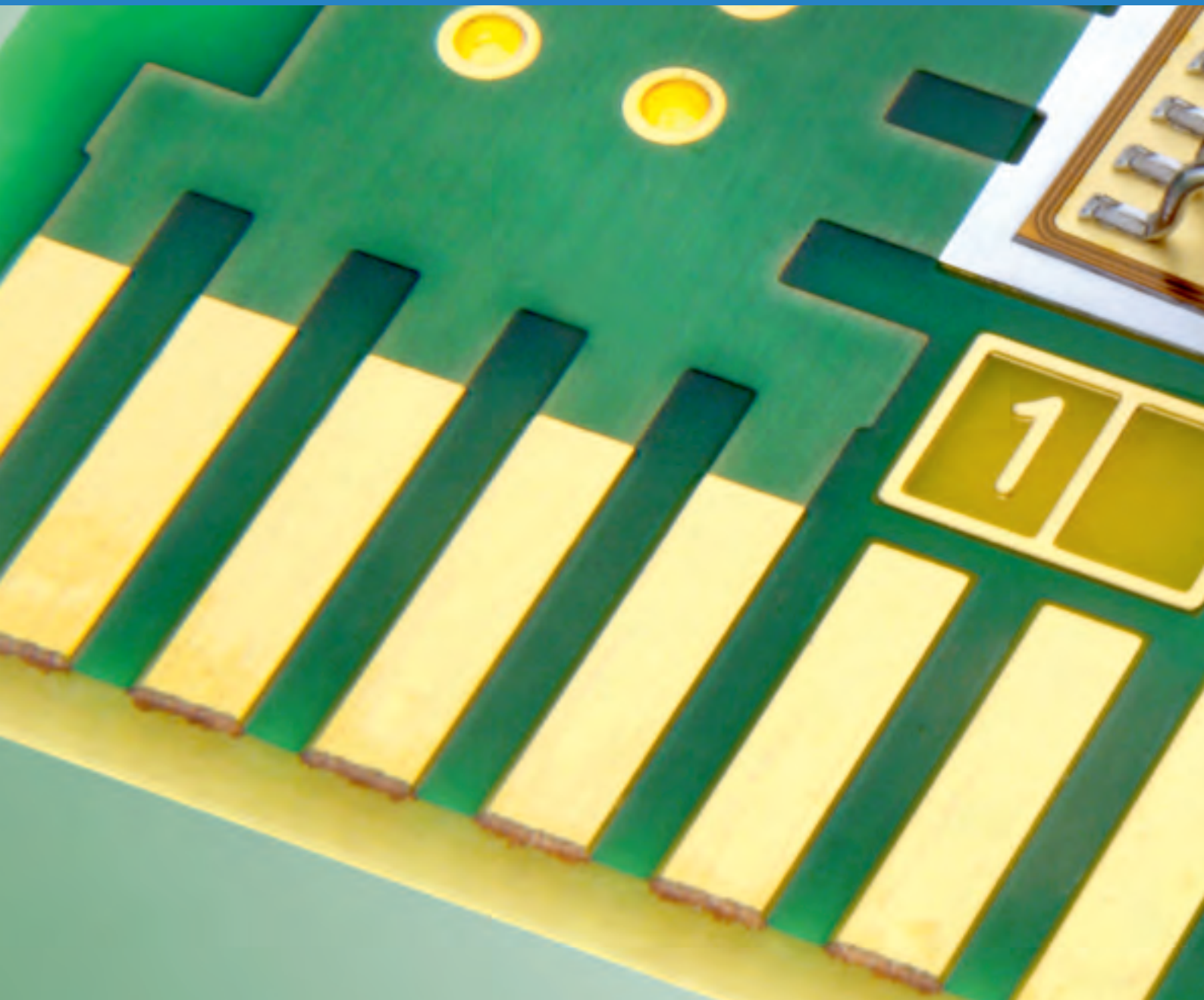
Key features

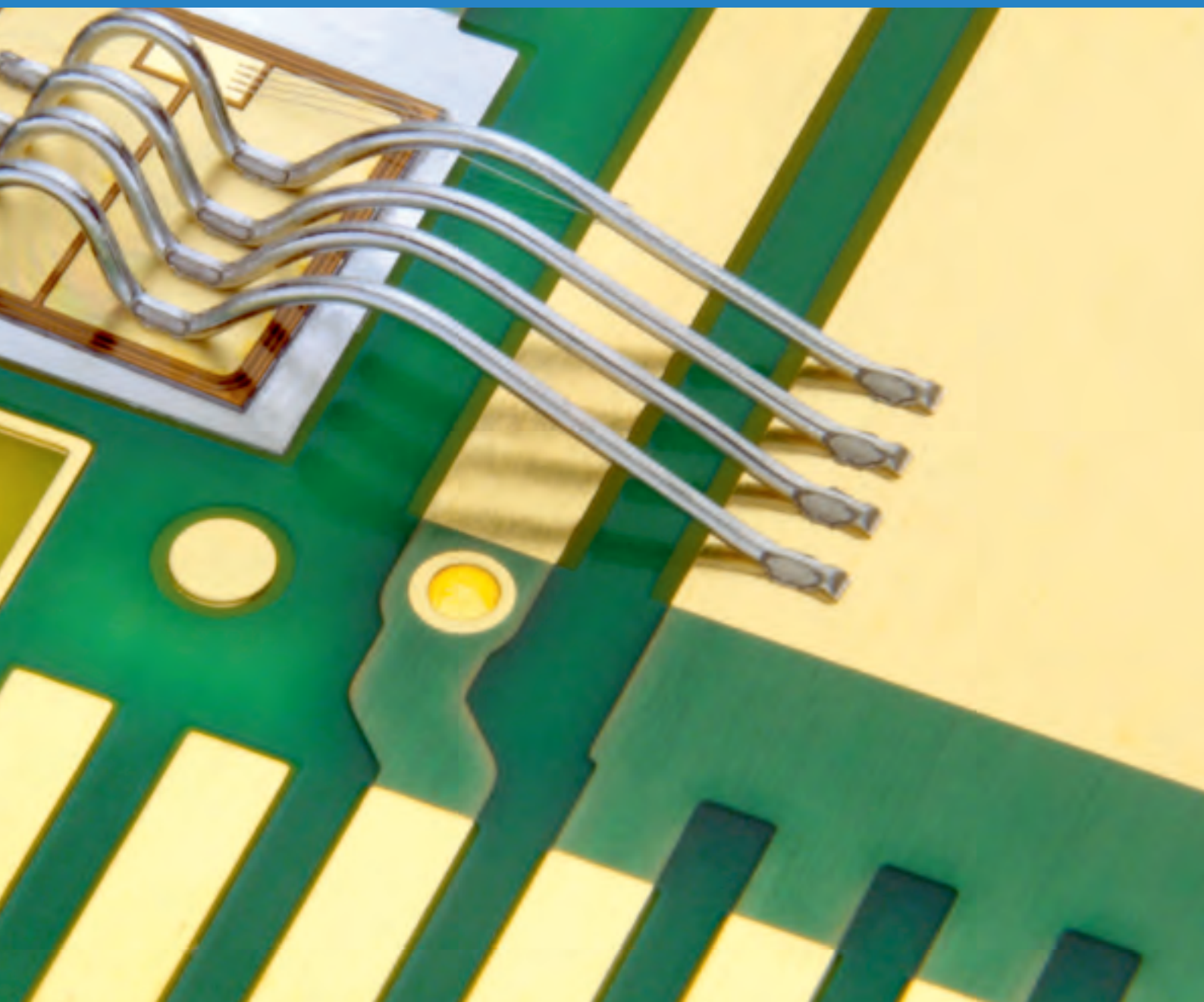
- 1,8 V / 5 V CMOS
- Fully isolated devices available
- NLD MOS up to 40 V
- Complementary Drain Extended CMOS (DECMOS) up to 40 V
- MiM capacitor and high-sheet poly resistor
- Embedded non-volatile memory
- Schottky diode and bipolar devices
- Standard 1P4M process, with up to 6M available
- Thick metal layer or copper plating for power routing

Located in South Korea, Dongbu HiTek operates two foundries with a cumulative capacity of 94.000 wafers per month, with focus on Analog and Mixed-Signal products. The foundry offers technology nodes from 0,35 μm down to 90 nm and processing technologies for BCDMOS, Analog and High-Voltage CMOS, Mixed-Signal, Flash and Logic applications.

REPRESENTATIVE RESULTS OF WORK

IC TECHNOLOGY AND POWER ELECTRONICS





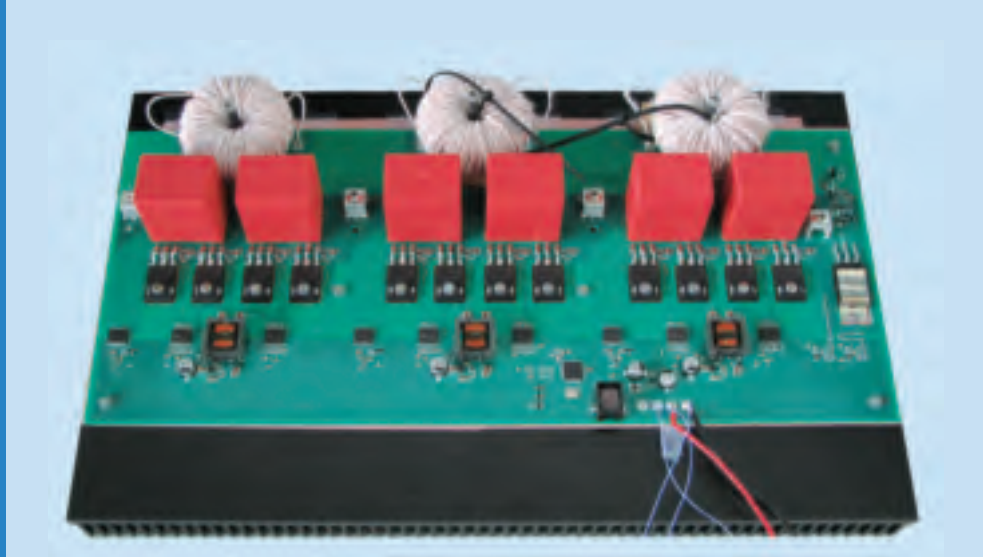


Figure 3: Realized, bidirectional DC/DC converter

FLEXIBLE AND SCALABLE BATTERY STORAGE SYSTEM WITH BIDIRECTIONAL DC/DC CONVERTER AND BATTERY MANAGEMENT FOR PHOTOVOLTAIC APPLICATIONS

Storing electrical power is necessary to support the decentralized electrical power supply and to reduce fluctuating loads on electricity grids. It is also economically reasonable for consumers with photovoltaic systems because of declining compensation for generated electricity. Particularly high efficiency on electricity grids can be achieved if the generated energy is stored locally and consuming devices are connected via an intelligent load management.

In recent years, a variety of photovoltaic (PV) generators was installed. The economic feasibility of domestic energy storage in advanced photovoltaic systems depends essentially on the

total efficiency of the electrical energy storage as well as on the necessary investment costs for retrofitting. Therefore, a battery module with low storage losses and long lifetime is required, as well as a comprehensive system solution which allows to reuse existing components.

The Fraunhofer ISIT developed a novel household energy storage module, connecting the battery pack at the DC side between the existing inverter and the photovoltaic array. With this development project, the Fraunhofer ISIT also gains system expertise in the field of power electronics applications. The concept is illustrated in figure 1: The battery storage system is connected via a bidirectional DC/DC converter to the DC voltage bus of the photovoltaic plant.

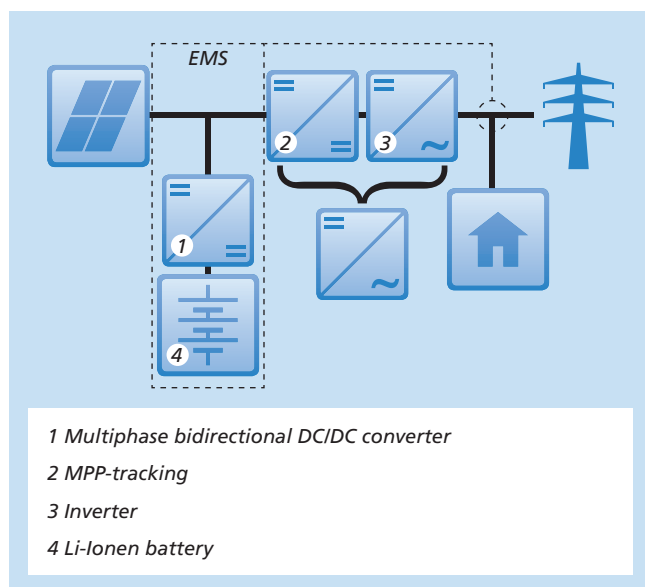


Figure 1: System concept with battery storage system on the DC side

The development of the DC/DC converter as an interface between PV and battery side should achieve optimal efficiency. Therefore, a battery storage system with scalable battery voltage was designed, where Li-Ion batteries, as well as Li-Titanate batteries with much longer lifetime can be used. As a prerequisite for long-term stability and high efficiency, a patented battery management concept was developed. It dynamically adjusts the battery voltage without losses and has a dynamic cell balancing on single cell level. The bidirectional DC/DC converter was built in MOSFET technology and has a very wide input and output voltage range from 175 V–550 V on the PV side and 175 V–488 V on the battery side. For choosing the topology, a particular emphasis was placed on a very high total and partial load efficiency to charge the battery also during low-light phases. This was achieved by a 3-phase, bidirectional H-bridge with a target efficiency of 98.5% at 20% load (figure. 2). Depending on the actual converted power, one to three phases are used to maximize the converter efficiency across the whole operating range.

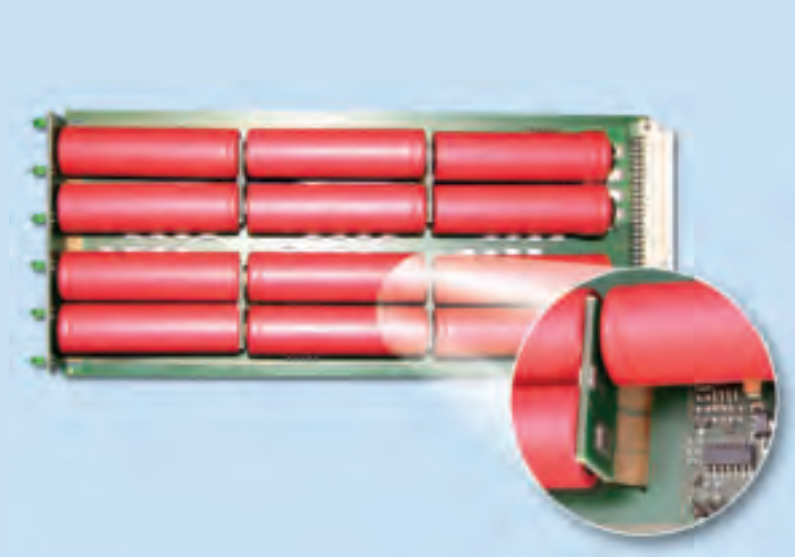


Figure 4: Realized battery slave board

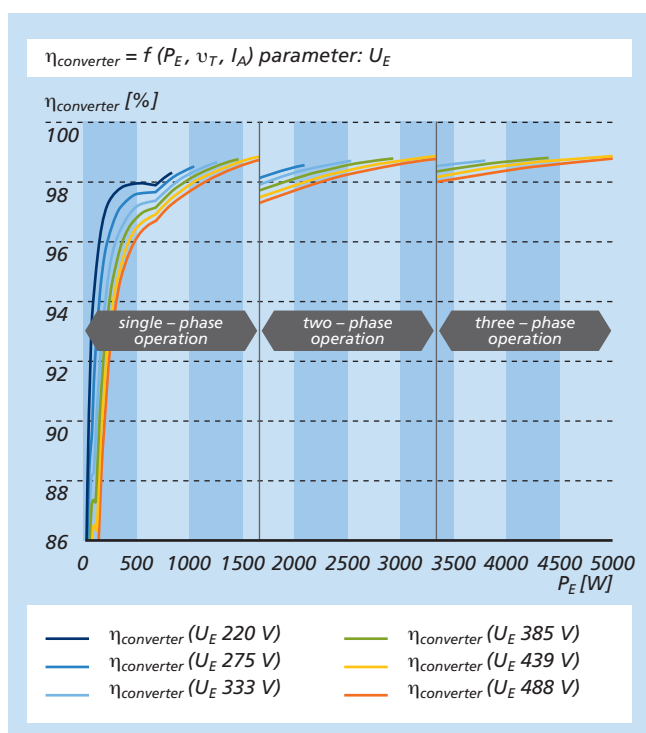


Figure 2: Target efficiency of the DC/DC converter

The DC/DC converter contains an innovative, highly dynamic control method with state space controller. The control parameters are adapted automatically for each actual operating point. This offers significant advantages for the dynamic behaviour, compared to conventional PI controllers. In addition, the DC/DC converter enables the storage system to be well compatible with the MPP (Maximum Power Point) tracking of solar inverters. It prevents an inappropriate power

point of the solar field in case of battery charging/discharging conditions. The realized DC/DC converter is shown in figure 3.

The next subsystem, namely the battery system, consists of one main controller and a large number of slave devices, i.e. one for each block of cells. The high amount of cells in series supports a variable battery voltage level. Each of these slaves may be employed or bypassed as requested by the main controller. This feature enables a loss free dynamic cell balancing, just by bypassing degenerated cells with incorrect cell voltage. Since this method is very effective, even cells which are degrading over time may be kept in the battery pack without large influence on the whole system. In case a cell is really damaged, it will be bypassed all the time, without any influence on the overall functionality. Due to this behavior, the battery system is very reliable and fault tolerant. Furthermore, the main controller can adjust the number of cells in the battery string dynamically to achieve a battery voltage which fits well to a high efficiency operation of the DC/DC converter (figure 4).

The entire system of solar inverter, DC/DC converter, storage batteries and PV array is controlled by an integrated energy management, which focuses on the actually used line current and not only aims at a maximum state of charge for the battery. Line current and voltage are easily measured by a few sensors. The control mechanism minimizes the current consumed or supplied by the power grid according to the SOC (State of Charge) of the battery. To increase the operational efficiency, the energy management chooses an optimal battery voltage, which is a special feature of the patented battery management system.

The Fraunhofer ISIT is planning to use application specific Li-Titanate batteries for increased efficiency and long lifetime.

MODERN METALLIZATION PROCESSES FOR POWER COMPONENTS

Energy efficiency and long time reliability are the main topics for new power packing technologies. This objective is backed by state of the art power devices with minimized energy loss for both, on-state and fast switching. Since heat generation within power components is not completely avoidable, the heat transfer to a coolant must be optimised in order to keep the junction temperature of the devices low. In addition, the space for power modules is restricted in most applications. Therefore, power modules are supposed to be as small as possible, to work at highest power density, and of course to perform for a very long time without failure. Among other technical aspects, modern front-side metallization stacks and alternative connection technologies enhance the heat flow on both sides of the power components towards the heat sink.

Power devices usually are soldered or sintered with their bottom contact to a metalized ceramic plate. This ensures good electrical and thermal contact of the device and enables the transportation of heat directly to the coolant. Aluminium-oxide (Al_2O_3) is the commonly used ceramic plate material in most standard products, while aluminium nitride (AlN) or silicon nitride (Si_3N_4) substrates are particularly suited for high-power modules. The latter materials show a lower thermal expansion coefficient and a higher thermal conductivity. A

number of technologies are in use for attaching metal to the various substrates, utilizing melting and diffusion or metal brazing. According to the procedure used, Direct Bonded Copper (DBC), Direct Bonded Aluminium (DBA) or Active Metal Brazed (AMB) substrates are available factory-made. A frequently used bottom metallization of power devices (collector or drain) is based on a sinterable or solderable nickel/silver (Ni/Ag) metal stack. In contrast, the front side metallisation (emitter or source, and gate) is typically made by sputtered aluminium (Al or AlCu). In case of aluminium based contact areas, the electrical interconnection between DBC substrate and the device's front-side metallization is realized by aluminium wire bonds, which is a widely applied standard technology.

A disadvantage of bond wires is that they will not improve the heat dissipation, since the number of wires and their diameter are restricted. The thermal load is unfavourable for the mechanical stability of aluminium (Al) wires and they show degradation in the long run. The use of copper (Cu) instead of Al would improve the reliability of the substrate-to-die interconnection since it shows better mechanical and electrical property as well as an increased thermal conductivity. Since copper wires can not be bonded to Al surfaces, a chip metallization with Cu is required.

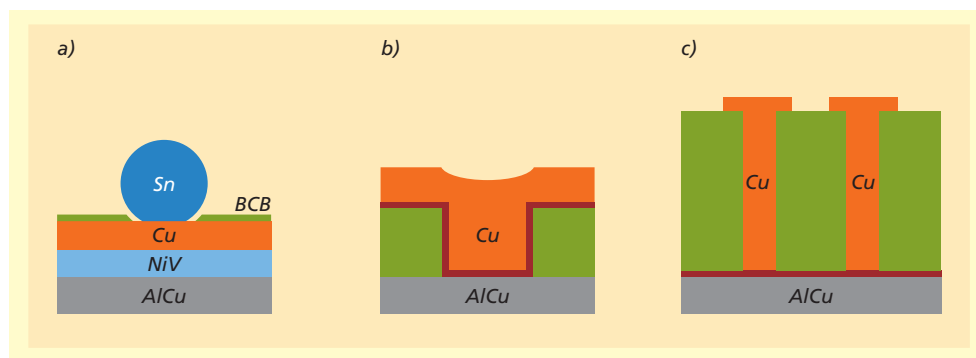


Figure 1: Schematic illustration of various front-side under-bump metallisations.
 a) Solder ball placing and reflow
 b) Cu through-hole plating
 c) Cu pillars or micro-posts



Figure 2: IGBT wafer supplied with Cu UBM and solder balls

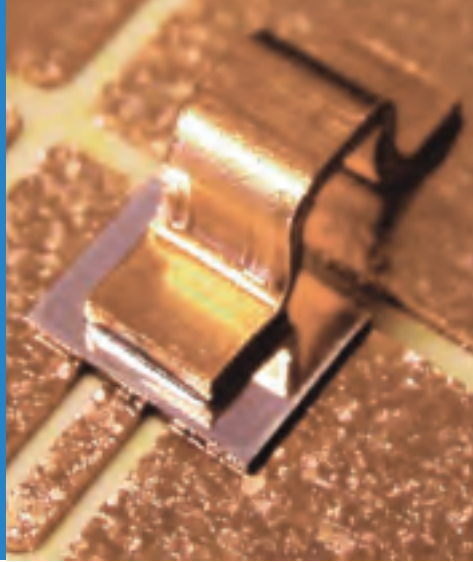


Figure 3: Solder-bumped IGBT as shown in figure 2, now soldered upside down to a DCB ceramic test board. The collector contact is made by Cu-clip

This is also the case for the use of copper ribbon bonding which is increasingly done for interconnecting Insulated Gate Bipolar Transistors (IGBTs) on DBC-substrates. The advantage of metallized copper terminations implies a growing demand for front-side metallization processes with Cu as top layer.

In the following, some metallization concepts are outlined which have been evaluated at Fraunhofer ISIT in conjunction with other research projects.

Device Termination Using Cu as Top Metallization Layer

The schematic illustration in figure 1(a) shows the cross section of a typical front-side under-bump metallisation (UBM) stack which is supplied with solder balls of about 300 μm in diameter. At first, AlCu and Nickel-Vanadium (NiV) are sputtered, then copper is deposited on top of the nickel layer. The copper would act as base layer for the solder ball placement. Prior to the solder-ball placement, the Cu surface is structured by means of photosensitive BCB (benzocyclobutene) or comparable films (e.g. patterned polyimide) that will serve as soldering stop and electrical insulation. An IGBT wafer section after subsequent flux printing, solder ball-placing and reflow is shown in figure 2. These IGBT chips were successfully assembled by soldering them upside-down to a suitable Direct Copper Bond (DCB) test substrate, as shown in figure 3. The coupling between the IGBT bottom and the DBC ceramic was realized by Cu clip bonding. First tests showed that, due to the improved heat transfer, a higher current can be driven through the IGBT at stable saturation voltage (V_{sat}).

Figure 1(b) is depicting an example for a through-hole plating process with copper metallization. The contact openings are defined by patterned insulating films (e.g. BCB or polyimide). The plating is continued until the contact hole and the whole surface are covered with sufficient metal thickness. The

material used for patterning the contact area remains underneath the metal coating, thus it has to withstand subsequent processes like soldering.

An alternative process is the plating of metal pillars (or micro-posts) as shown in figure 1(c). In this case, also photoresist can be used for pattern definition since the removal of the resist prior to hot processes remains possible. The height of the pillars is defined by the thickness of the resist. Galvanic plating processes can be applied for filling the pattern. This kind of Cu pillar structure can be used for interconnecting the power devices to DBC substrates.

Application Specific IGBTs for New Assembly Techniques

The development of small and compact power modules with a direct cooling of the substrate is the intention of the BMBF founded project "Ultra-Compact Power Modules" (UltiMo). Power components (IGBTs and diodes) are supposed to be sandwiched in-between a top and bottom substrate. In figure 5, a cross section scheme is shown for one IGBT chip in such a sandwich assembly.

Hereby, the gate and the active area of the IGBTs as well as its bottom contact are either soldered or sintered to the DBC-substrates for the purpose of optimizing the heat transfer throughout the DBC cover to the coolant. The substrates used for the modules are themselves not thermally connected to a base plate, because they are cooled directly by e.g. water/glycol, oil or air. Due to this enhanced cooling concept, a higher output power is allowed, the ampacity of the device can be increased while the junction temperature is kept low. Connection techniques like "direct soldering", "liquid phase bonding" (LPB) or "sintering" of particularly both sides of the device are expected to be beneficial for the heat transfer and the reliability of modules. After merging the substrates and

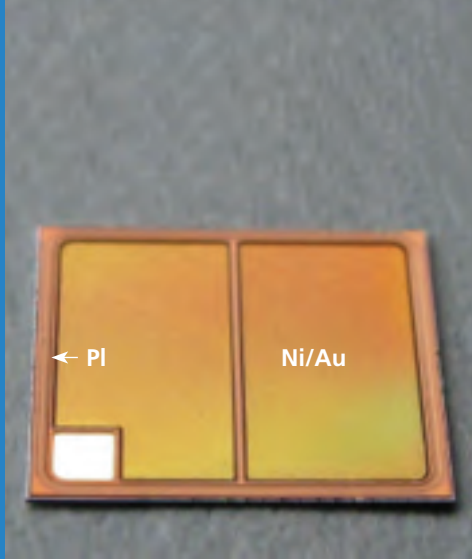
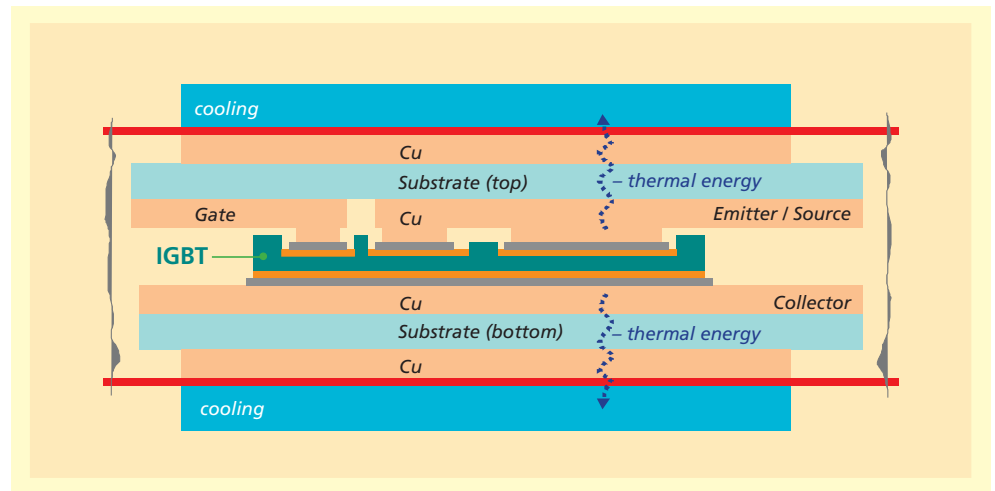


Figure 4: Field-stop IGBT (600 V / 75 A, 70 μm thickness) with electroless plated Ni/Au termination; the metallization is surrounded by PI

Figure 5: Cross section of an „Ultra-Compact Power Module“ sandwich assembly of DBC-substrates and corner gate IGBTs. All IGBT terminations are sintered or soldered to copper coated ceramic substrates



the chips, a special designed encasement is built around the assembly for protecting them against environmental influence.

Components with sinterable or solderable front contacts are not yet commercially available off-the-shelf. For that reason, the technology for 600 V / 75 A IGBT devices has been developed at Fraunhofer ISIT including specific types of front side metallisation schemes that are designed to fulfil the requirements of modern assembly concepts.

In the following, IGBT surfaces will be shown with either Ni/Au, Ni/Ag or Cu/Sn front side termination. In all cases, the IGBTs are covered with photosensitive polyimide (PI) of 20 μm thickness, which has been measured after performing the processes for photolithography and final curing at 350°C. Thereafter, the AlCu surface of the gate and emitter termination can be coated with the desired metal stacks.

A nickel and flash-gold (Ni/Au) metal stack can easily be deposited within the polyimide openings by use of an

electroless plating process. In figure 4, an IGBT chip with Ni/Au metallization is shown, a schematic cross section for this metallization is displayed in figure 6 showing a metal stack of AlCu/Ni/Au with flash-Au (70 nm) as top metallisation.

In contrast to the electroless plating process, a metal stack of titanium/nickel/silver (Ti/NiAg) is evaporated all over the wafer

Figure 6: Schematic illustration for electroless plated Ni/Au (2 μm / 70 nm)

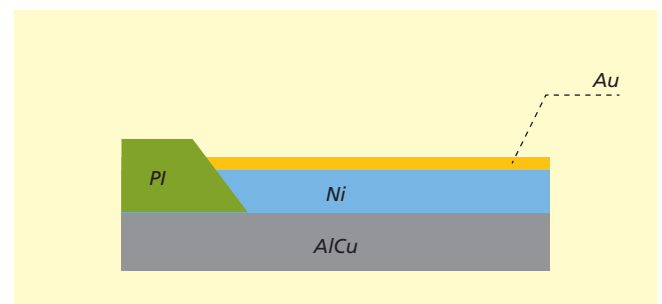




Figure 7: Trench IGBT with Ni/Ag termination

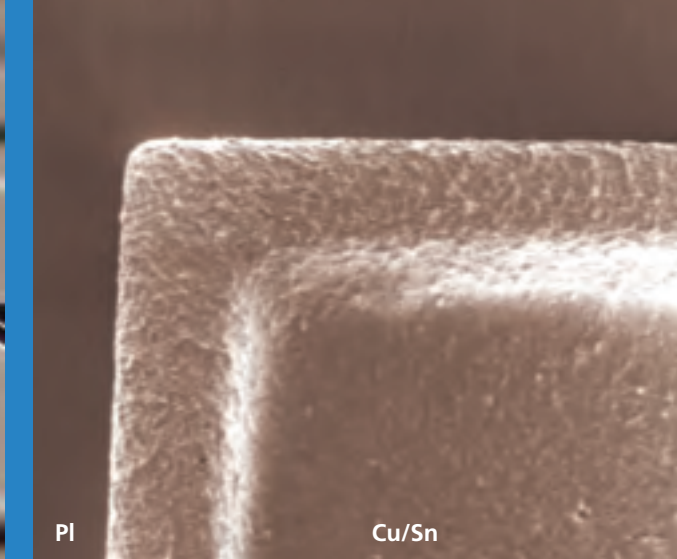


Figure 8: The Cu/Sn edge covering is shown in this SEM photograph

and must finally be structured layer by layer, employing photolithography and wet chemical etching processes. The metals are extending to the polyimide top as illustrated in figure 9. A view onto an IGBT wafer surface after Ti/Ni/Ag structuring is given in figure 7.

In case of applying galvanic plating processes for the copper and tin (Cu/Sn) deposition, a top metallization is achieved as illustrated in figure 10. Also in this case, the plating is extending to the top of the polyimide insulation. The photograph in figure 8 was made by use of a scanning electron microscope (SEM). It shows the edge covering with Cu/Sn extending from the IGBT termination onto the top of the polyimide.

The project "Development of customer-designed IGBTs for both side solder- and sinterable assembly technologies" is funded by the Federal Ministry for Education and Research (BMBF) within the project UltiMo as part of "Leistungselektronik zur Energieeffizienz-Steigerung" (LES), conveying program "IKT 2020".

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Figure 9: Schematic illustration for evaporated Ti/Ni/Ag on AlCu after wet etching

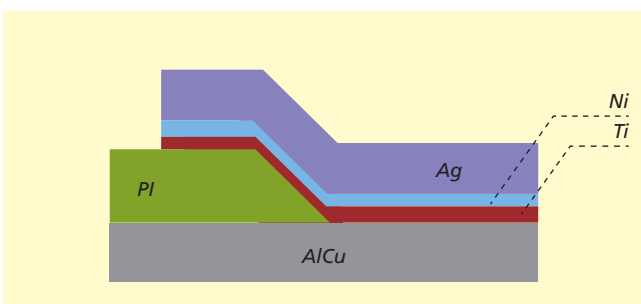
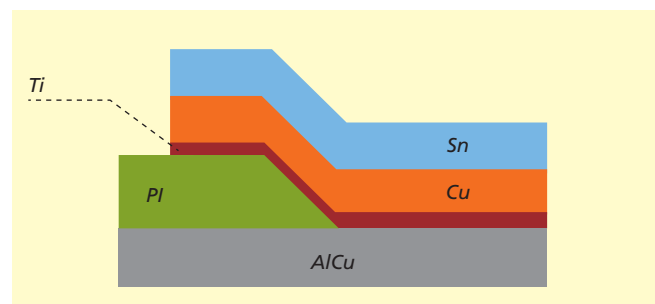


Figure 10: Schematic illustration for electroplated Cu/Sn on Ti/Cu plating base



HIGH-VOLTAGE POWERMOS: NEW COMPENSATION DEVICES BASED ON THE SUPER JUNCTION PRINCIPLE

Fraunhofer ISIT is investigating new technologies for the fabrication of high voltage compensation PowerMOS devices with improved energy efficiency. For PowerMOS transistors, the reduction of the on-state resistance $R_{DS,on}$ is still the most important R&D topic. The main contribution to $R_{DS,on}$ is the serial resistance of the transistor's drift zone which defines the so-called silicon limit. The most striking feature of all compensation devices is the capability to overcome the silicon limit. Thus, compensation devices like the p-n junction transistor COOLMOS (Infineon) were developed, but the production of COOLMOS devices is time-consuming and cost intensive. Therefore, Fraunhofer ISIT is investigating a new technology for the production of p-n junction transistors. The principle of a p-n junction device (also known as Super PowerMOS) is depicted in figure 1. Each of the n-type transistor cells is bordered by p-type compensation structures. These structures were etched and filled by single layer epitaxy. Common compensation devices use a multi-layer epitaxy and implantation process to create the compensation device. The material within the trenches is doped in such a way that it is acting as compensation structure. In the off-state of the PowerMOS device, the doping of the p-type column is allowing a two-dimensional depletion of the drift zone. This effect can be utilized to increase the doping concentration of the drift zone, which is beneficial for the $R_{DS,on}$.

Simulation

By use of this advanced technology, Fraunhofer ISIT has fabricated high voltage diodes and transistors in order to demonstrate the compensation effect. The whole device including the compensation structures has been simulated by use of a commercial process and device simulator (ATLAS). To account for the difference between simulation and semiconductor process technology, the distance between the compensation trenches has been varied in a range from $3.5\ \mu\text{m}$ to $4.5\ \mu\text{m}$, which is also the width of the transistors. The variations would allow to localize the point of complete compensation of the transistors under given circumstances. At a transistor width of $4.0\ \mu\text{m}$, the simulation tools calculated a breakdown voltage of 200 Volts.

Because the electric field in compensation devices is higher than in standard PowerMOS devices, an appropriate termination had to be found that would accommodate these fields. The best result in our simulations was the so-called

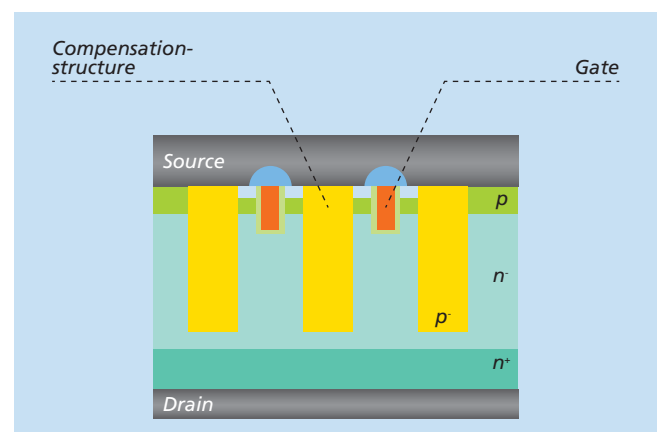


Figure 1: Principle schematic of a PowerMOS device surrounded by compensation structures

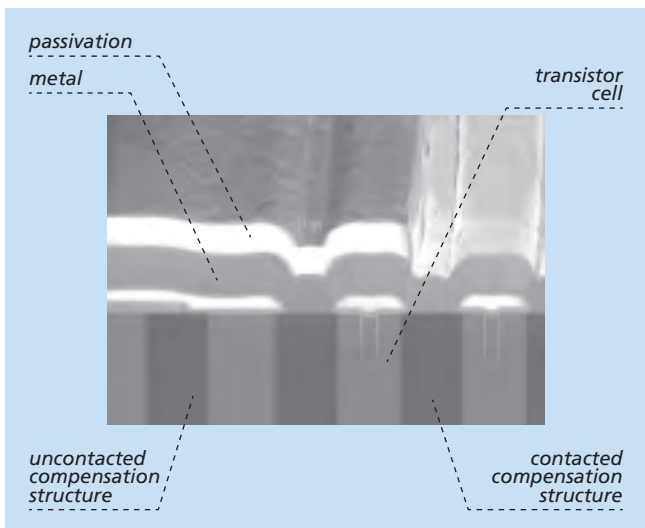


Figure 2: Focused ion beam (FIB) cross section of a completed wafer, the compensation structure is colored darker to show position and size

extension termination: The extension termination is a low-doped and shallow implanted p-region placed between uncontacted compensation structures. These structures are shown in figure 2 on the left side of the picture. On the right side, two transistor cells with contacted compensation structures are to be seen. All compensation structures that are encircling the MOS transistor are contacted at their upper interface to the source contacts.

Technology

For fabricating the compensation structures, a new deep trench etching process was implemented. This process has a special trench profile and generates a smooth trench wall. Both qualities are required for a void free trench filling. The trench filling was optimised by a newly developed sequential process. The process comprises boron doped (n-type) epitaxial silicon growth and etch-back of excess silicon depositions from the trench walls. The epitaxial silicon growth was performed under low pressure. These sequences enable a void free filling of the trenches. Chemical Mechanical Polishing (CMP) is used for the planarization of the trenches to achieve a topology of less than 20 nm. All processes following CMP are standard technology steps commonly used for the production of PowerMOS devices.

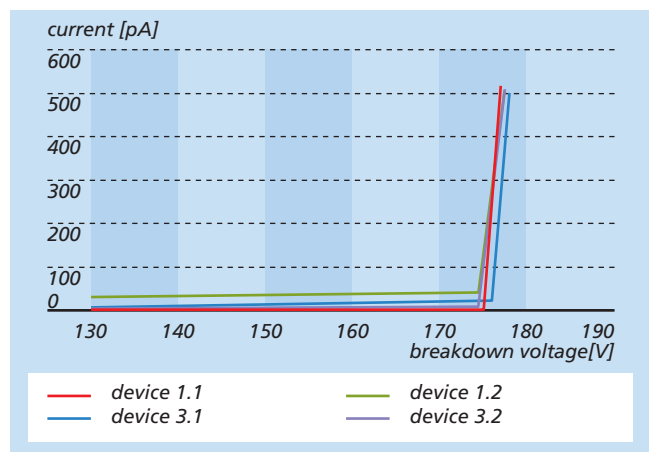


Figure 3: Breakdown voltage of high voltage PowerMOS Super Junction transistors on different wafers

Results

First results confirm the feasibility of the single layer epitaxy approach for super junction devices. A breakdown voltage of 180 Volts for compensation devices was achieved. Figure 3 illustrates the forward off-state current vs. the breakdown voltage for different devices. The target value of the measured breakdown voltage of about 180 Volts could be reached. Without compensation, a breakdown would happen approximately at 100 Volts. A typical drain current vs. drain voltage (I-V) output characteristic is shown in figure 4 for different gate voltages (Vg). For the data displayed in figure 4, the $R_{DS,on}$ could be calculated to a value of $4.6 \text{ m}\Omega\text{cm}^2$ for a gate voltage of 15 Volts. This $R_{DS,on}$ value is typical for a PowerMOS device with a break down voltage of about 100 Volts.

Main objective of further optimisations is increasing the break down voltage up to 400 Volts.

The R&D work was first carried out within the BMBF project "Energieeffiziente Leistungsbaulemente für den Spannungsbereich bis 400 V" at ISIT and is continued as a major research project.

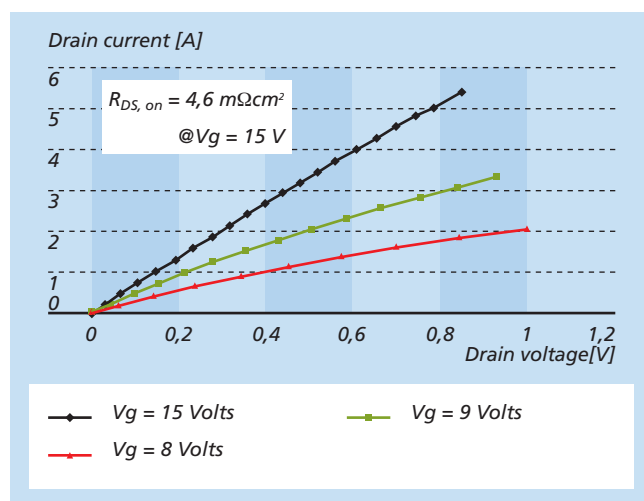
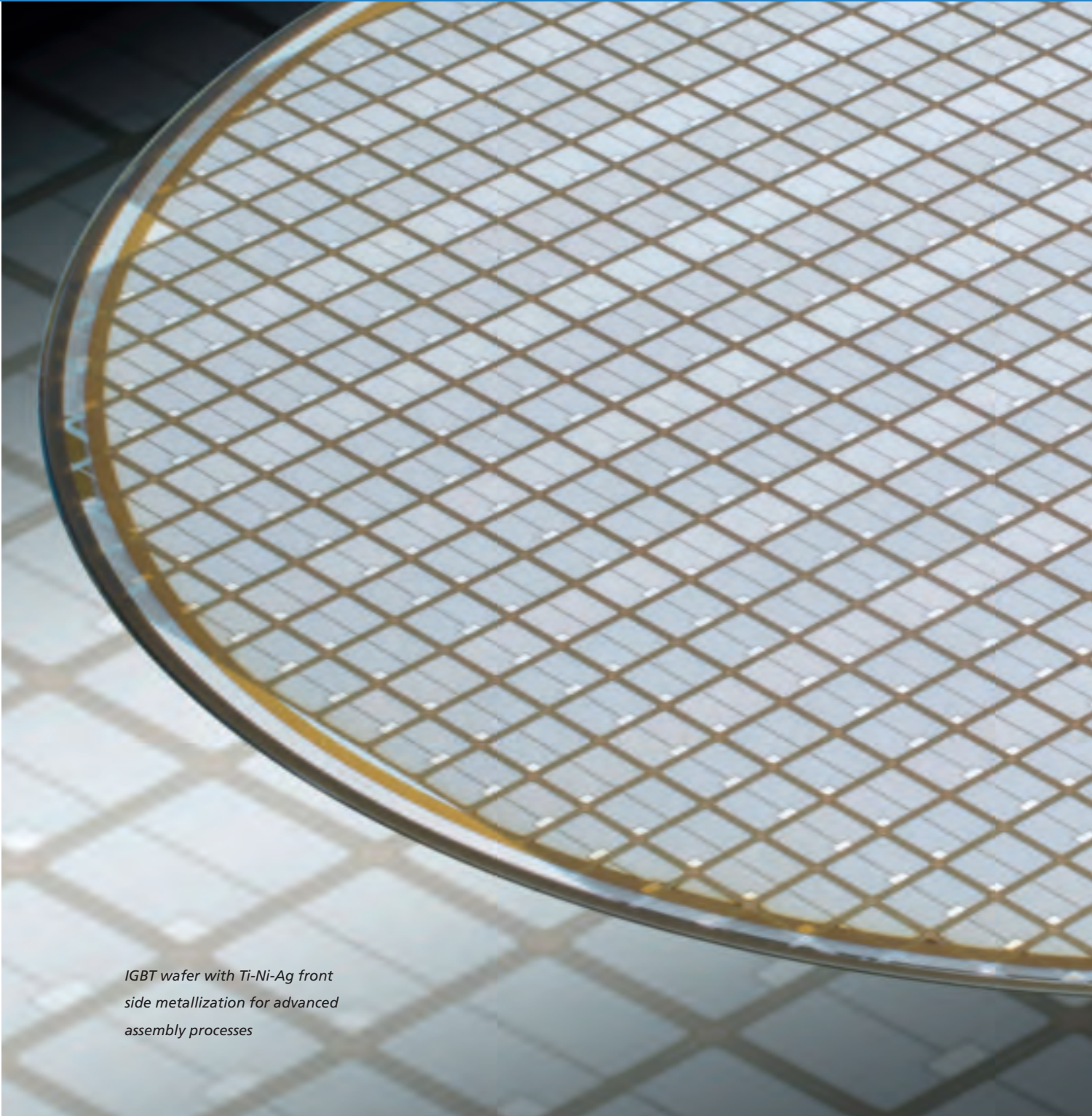


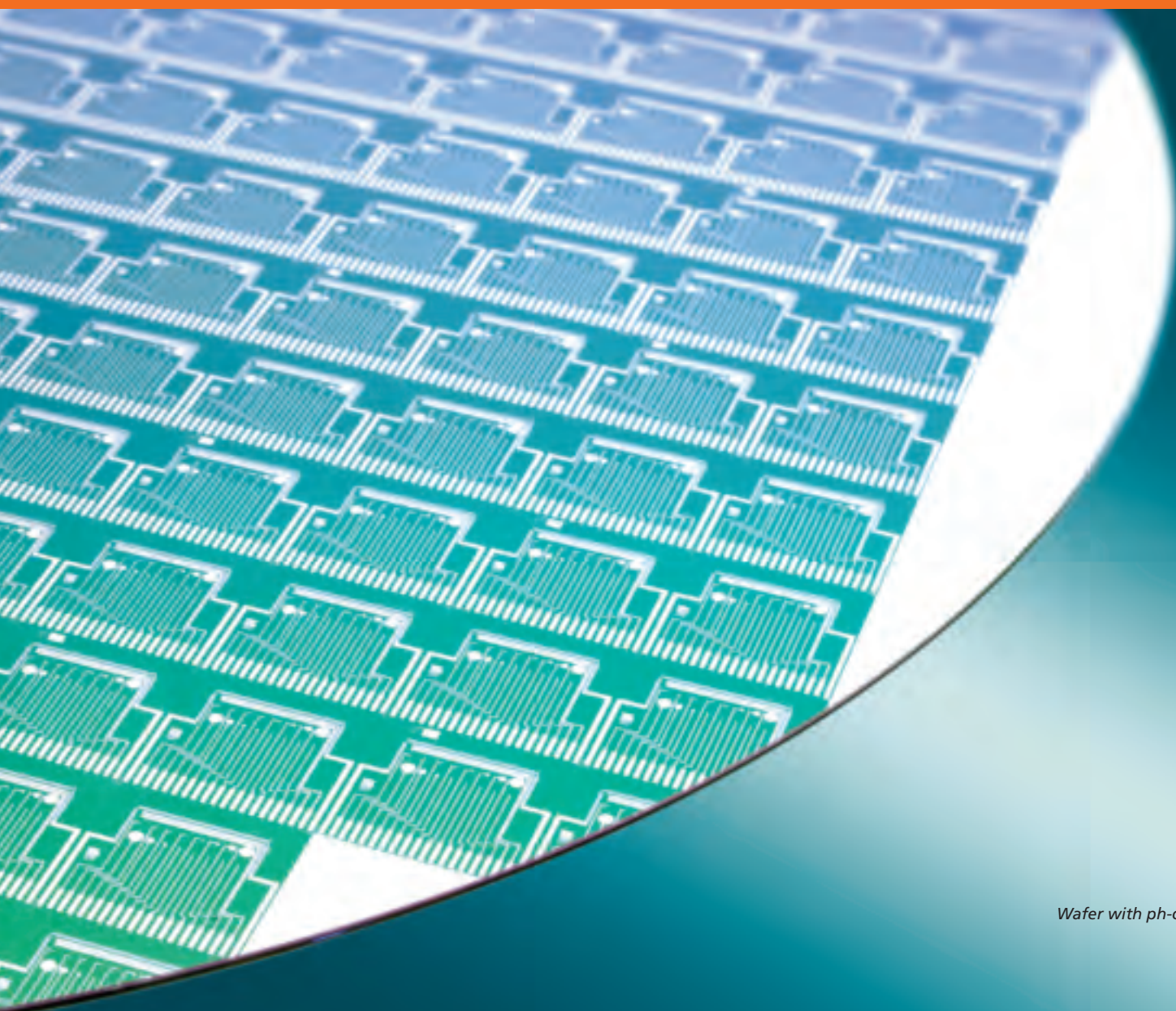
Figure 4: Output characteristics of a Super Junction device for different Gate-Source voltages



IGBT wafer with Ti-Ni-Ag front side metallization for advanced assembly processes

REPRESENTATIVE RESULTS OF WORK

BIOTECHNICAL MICROSYSTEMS



Wafer with ph-chips

MEMBRANES AND MICROELECTRODES FOR CELL-FREE BIOPRODUCTION

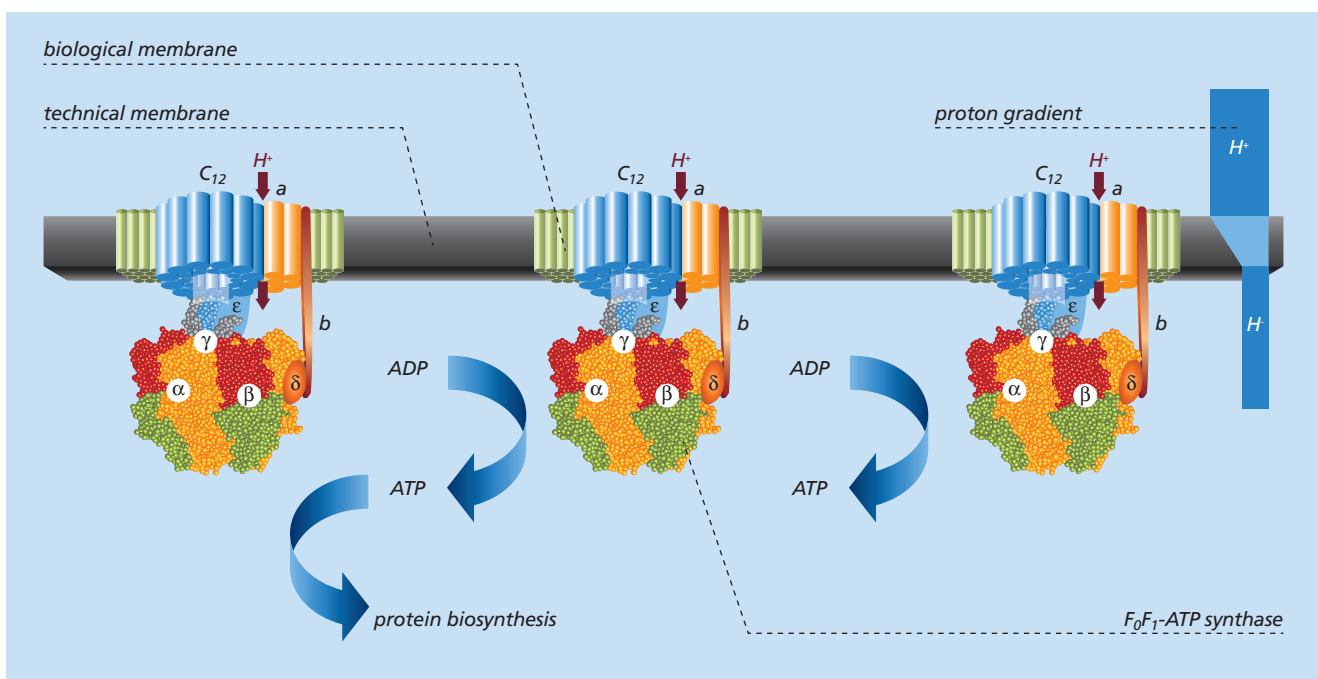
The market for native and complex proteins, e.g. enzymes, is large, especially in pharmaceutical, food and cosmetics industry. Currently the industrial production of proteins is done in living cells, although in these systems the yields are insufficient, the extraction of the proteins is laborious and therefore the economic efficiency is limited. Further, the production of toxic proteins is often hindered, because the cells are killed by their products.

As an alternative to cell-based systems, cell-free bioproduction was established in recent years. The synthesis of proteins in cell lysates leads to a better efficiency by good mass and time yields, easy protein extraction and the possibility to generate toxic molecules.

With the aim to make cell-free bioproduction compatible to an up- or down-scalable mass production technology, a Fraunhofer consortium was founded. Eight Fraunhofer institutes are participating in this consortium: IBMT, IZM, IGB, IPA, IPK, IME, ISI and ISIT. The Fraunhofer Gesellschaft is spending 6 million Euros for the project "Cell-Free Bioproduction" in the framework of their systems research. This sum is complemented by 14.5 million from the Federal Ministry of Education and Research (BMBF) as a part of the Biotechnology 2020+ strategy process.

The aim of the project is the cell-free protein production with integrated energy supply. The main tasks are to develop reactor systems for continuously controllable

Figure 1: Scheme of ATP pore membrane



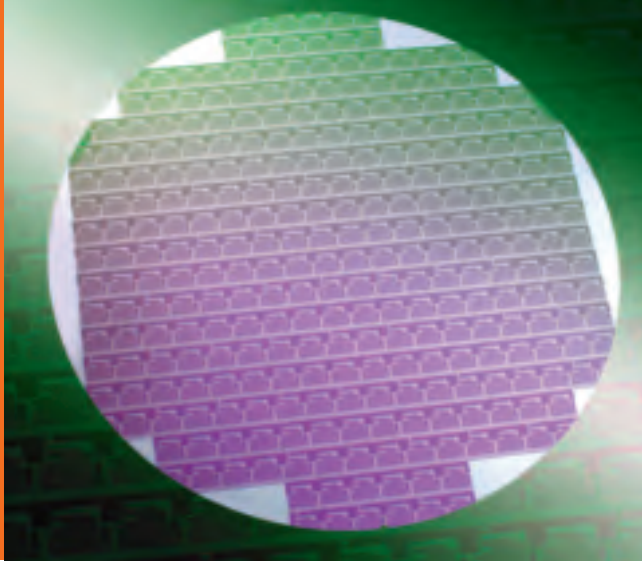


Figure 2: Wafer with Iridium oxide electrodes in different dimensions

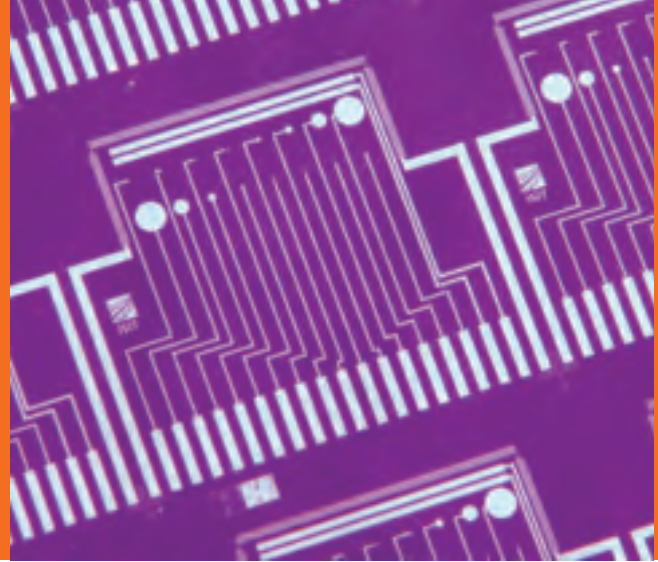


Figure 3: Sensorchip with pH sensitive electrodes

cell-free synthesis of biomolecules, essential elements for continuous production of biochemical energy in form of adenosine triphosphate (ATP) as well as to determine process conditions in terms of quantity and robustness for industrial needs.

ISIT's contribution within the consortium is defined according to the competences in sensor and microsystem technology. It includes the construction of a silicon membrane chip for the development of the energy module (ATP module) within the reactor system. The membranes are very thin and contain thousands of nanometer-scaled pores. Across this net of pores, the enzyme ATP-Synthase for the biochemical energy supply within the reactor will be embedded in a double-lipid-layer, mimicking the membrane of a mitochondrion. ATP-Synthase regenerates the energy molecule ATP out of adenosine diphosphate (ADP). To activate the enzyme, a proton gradient has to be provided across the membrane. This gradient will be monitored by measuring the pH-value of the solutions on both sides of the membranes. The pH-measurement will be realised by integrated microelectrodes made out of iridium oxide.

Membrane Production

A silicon based approach of a chip for carrying bio membranes with the following parameters was designed:

- silicon wafer as base material with a technical membrane of silicon oxide
- chip size of 10x 10 mm to allow handling of the membrane and integration into test cavities
- membrane size 500x 500 μm with a thickness of around 2 μm
- different pore numbers between 16 and 10 000 in a variation of size in a range between 0,4 and 2 μm
- a gold layer on one side of the membrane for immobilisation of bio components via thiol coupling

For production of the wafers, different processes in ISIT's industrial silicon production environment were used, like high resolution photo lithography and reactive ion etching for structuring the pores and wet etching of silicon with potassium hydroxide (KOH) for building the membrane.



Figure 4: Electrical connected membrane sensor chip in a flow through reaction compartment

pH-Measurement

The microelectrodes for pH-measurement were also realised on silicon chips, which allows integration of such electrodes into small fluidic chambers of bio reactors. The electrodes were made of a metal stack with Tantalum as adhesive layer, a connecting layer of platinum and an upper active layer of Iridium. This Iridium layer was later oxidised by electrochemical treatment in diluted sulphuric acid on chip level. The Iridium oxide surface works as a pH sensitive electrode by giving voltage potentials proportional to pH-values. Critical parameters like sensitivity and stability of the sensor are validated by test series in different solutions. These solutions first consisted of standard calibration buffers and then were replaced by more project relevant solutions like lysates with different bio components. Especially these components are critical factors for stability of such sensors which in some cases requires further special treatment or even covering of the electrodes.

Miniaturization of the Electrodes for the Integration on Pore Membranes

A critical parameter of the pH-electrodes is size. For measurement of pH values in a whole compartment of a bio reactor, a size around 1 mm² is typically acceptable from integration size as well as regarding the electrical characteristics. Further miniaturisation is for example required for local measurement of pH on different positions of a membrane in an ATP-module. It is to be expected that reducing the electrode area lets the signal to noise ratio go down. For tests upon small electrode behaviour, special chips with varying electrode dimension were designed (Figure 3).

MODULE INTEGRATION

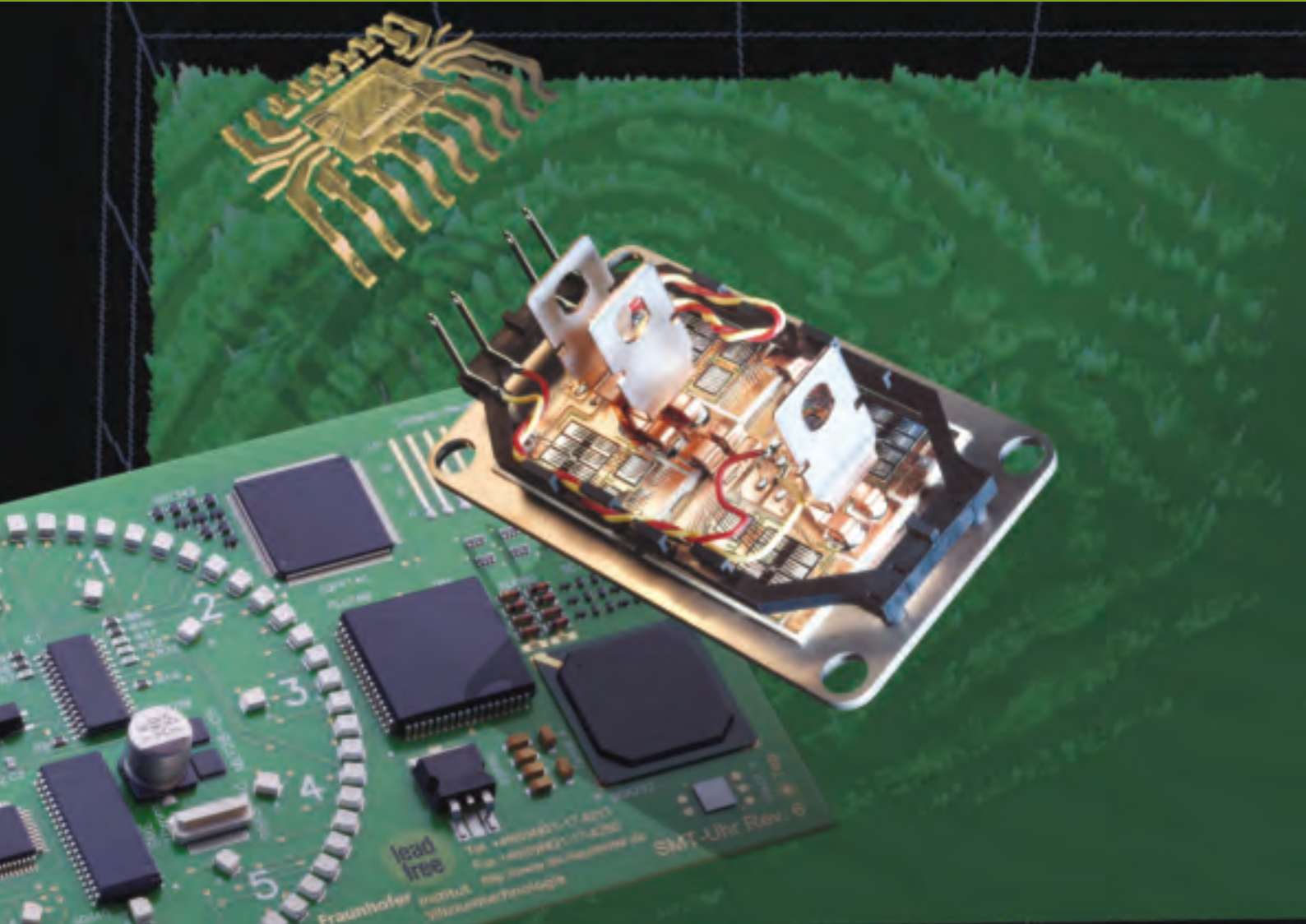




Figure 1: Left: Computer tomography system for 3D component inspection, right: 2D radiography system

NEW HIGH-RESOLUTION IMAGING TECHNOLOGIES AT FRAUNHOFER ISIT

The analysis and inspection of assembled and soldered electrical or microelectronic parts on PCB is of crucial interest to ensure failure-free function of electronic devices. Moreover, for avoiding future defects in these devices it is also very important to clarify reasons when modules show function failure.

However, the scale of integration increased while structure sizes decreased during the last years, and analysis techniques for destructive and non-destructive inspection have to keep up with these new challenges. Better resolution, higher contrast, high degree of measurement automation and the ability of handling and calculating huge data amounts in short times are only a few issues to be mentioned.

During the last years, Fraunhofer ISIT has consequently improved and assured its position in theoretical and practical knowledge for offering service and research in failure and damage analysis of electrical components. In this course, new state-of-the-art 2D radiography and computer tomography (CT) inspection systems as well as a high resolution laser profilometer have been acquired (figure 1).

Both systems allow non-destructive analysis accompanied by digital structure evaluation, i.e. void-solid ratio calculation and target-performance comparison. The fact that the analysed components are not damaged during inspection allows, for example, the application of rework or repair processes, which may save costs and efforts to the customer.

The information given by X-ray analysis is based on beam energy absorption caused by thickness and density variations in the investigated samples (figure 2).

With 2D X-ray inspection, also called radiography, fast and high resolution as well as high contrast analysis of samples with lateral dimensions up to 40 cm x 60 cm with tilted angles up to 70° is possible. Moreover, automated tray measurements and illumination recipe programming allow multiple probe measurements in short times. However, since there is only one beam direction in the 2D technique, only the totality of the absorption along the beam's path through the whole sample is visible in the obtained pictures, which may lead to uncertain results when evaluating e.g. the positions, directions or the extensions of local damages or embedded structures.

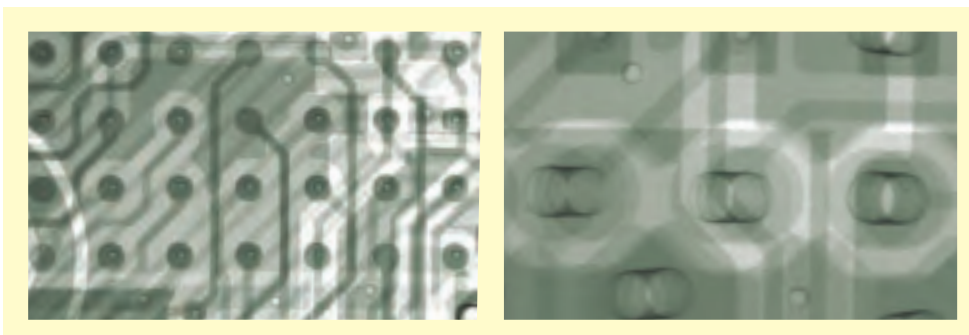


Figure 2: Left: Lines and microvias in solder pads for BGA soldering, right: Tilted view, inspection of via sidewalls

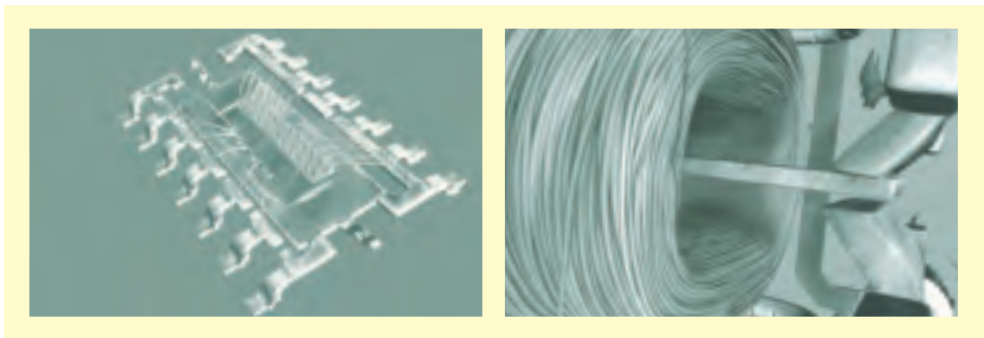


Figure 3: Left: CT of a standard IC. Right: CT of a relay coil

For more detailed inspection thus computer tomography (CT) is the better choice. In this technique, samples are mounted onto a glass rod or fixed into a circular holder and irradiated by X-rays with energies up to 180 kV under many (e.g. 360 – 2.400) different angles. Each angle results in a separate X-ray picture. Besides the sample position between the X-ray tube and the water-cooled CMOS ray detector, the electrical beam parameters and the number of angles determine the obtained resolution (min. 800 nm) as well as the resulting data amount and calculation time for beam reconstruction of the different angle pictures. For this, a high performance computer system has been installed.

Especially the CT system allows the extension of typical ISIT investigation fields like the analysis of standard components (figure 3), and of damage and solder connections of electrical components (figure 4) to the visualisation of material compositions such like of composites, foams (figure 5) and low absorbing laminates. A very specialty of CT is the creation of virtual cross sections without physical sample preparation or destruction. With this improved technique even the visualisation of very low absorbing materials or of their local embeddings (pores, voids, fibres, filaments etc.) like silicon, carbon, aluminium, ceramics or plastics is possible.

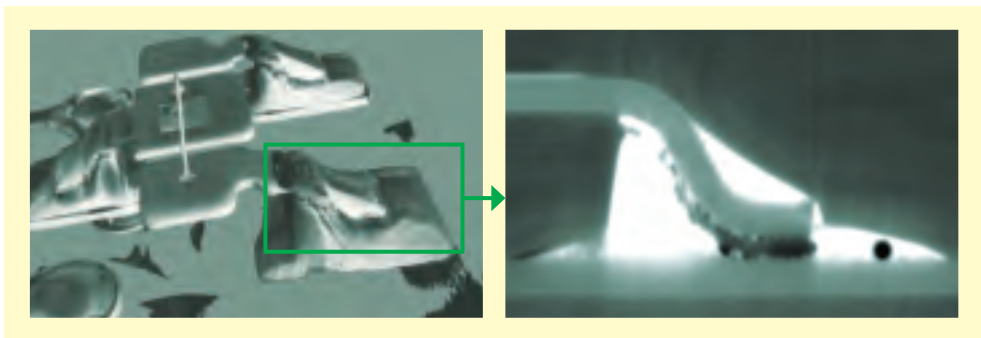


Figure 4: CT of a soldered SMD LED with obtrusive solder joints. Left: 3D overview, right: The virtual cross section shows a solder crack below the SMD pin

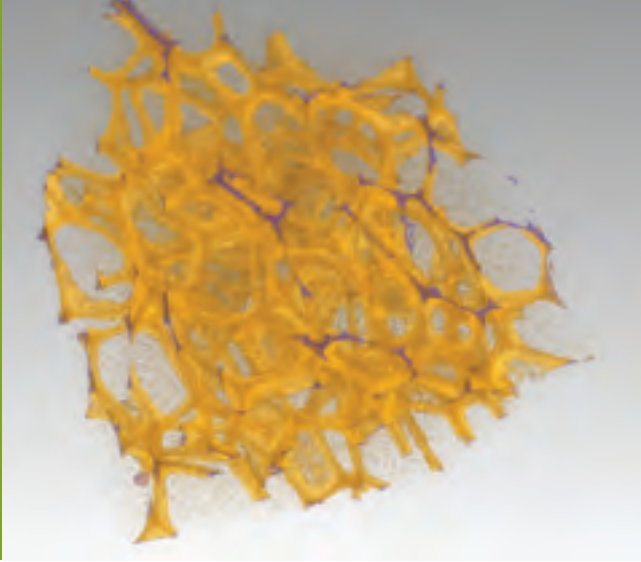


Figure 5: 3D picture after CT of a foam with colour encoded internal density variations



Figure 6: Surface analysis with optical laser profilometry

However, for obtaining definite and eye-visible results, ISIT is still performing physical sample treatment like cross section preparation and polishing as well as focused ion beam preparation and their further analysis for example with scanning electron microscopy (SEM) and energy dispersive X-ray fluorescence (EDX). A supplementary technique for non-destructive volume inspection by radiography is the analysis by ultrasonic microscopy which allows the visualisation of material (density) transitions like layer delamination, failed solder connections or cracks with z-resolutions down to ~ 20 nm.

A further new analysis tool for precise surface profile measurement is the new optical laser profilometer which applies the dual focus confocal measurement principle (figure 6).

Like in CT analysis, extensive post-processing options allow digital data reconstruction and evaluation, like roughness analysis, step height, curvature measurements and many

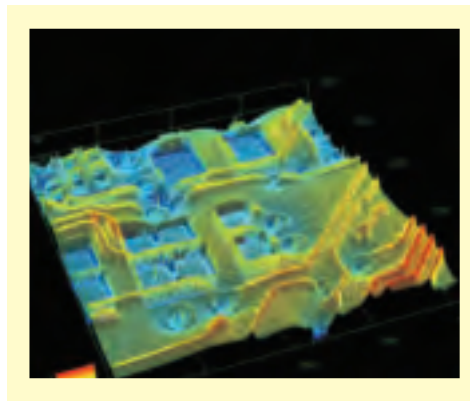


Figure 7: Height profile of a PCB surface. Below the solder stop lacquer layer the copper lines are visible

more. With physical magnifications ranging from 25 to 4.000, typical application fields are the geometrical evaluations of solder meniscus, PCB surfaces (figure 7) MEMS structures, periodical or random particle or residues distributions (figure 8), optical (also anti-reflex glass) surfaces (figure 9) and lacquer thicknesses calculations. Resolution limits are 120 nm in lateral and about 15 nm in z-direction, respectively.

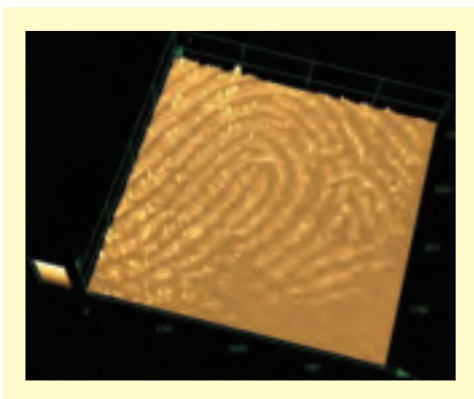


Figure 8: Fat and residues distribution, caused by a fingerprint on glass

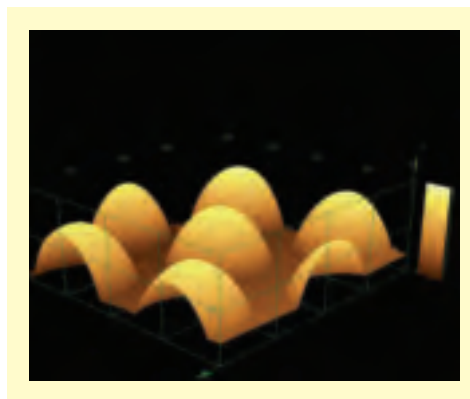


Figure 9: Cut out of an array consisting of aspherical microlenses

ADVANTAGES OF DOUBLE-SIDED COOLING CONCEPTS FOR POWER SEMICONDUCTORS – A PARAMETRIC STUDY OF THE INFLUENCE OF CHIP MOUNTING DETAILS ON THE JUNCTION TEMPERATURE

Introduction

Conventional power semiconductors are joined on their entire back side by soldering or sintering to a DBC substrate (DBC = Direct Bonded Copper) in order to achieve good heat dissipation. The semiconductors top side is electrically contacted by means of wire bonds which do not provide a significant heat dissipation path. A large area joint on the power semiconductors top side by soldering or sintering to a second DBC reduces the thermal resistance and increases the thermal mass adjacent to the chip. The latter is advantageous in case of pulse loads being significantly shorter than 1 s. Since the semiconductors top side cannot be contacted at the entire surface due to the gate contact and isolation requirements, cooling both sides will usually not result in half of the thermal resistance. Instead, it is typically reduced by about one third, which is equal to an additional heat dissipation of about 50% via the top-side connection. The position of the semiconductors top side contact areas may have an unfavorable influence in particular on the temperature distribution on the chip. These effects are described with the following model calculations.

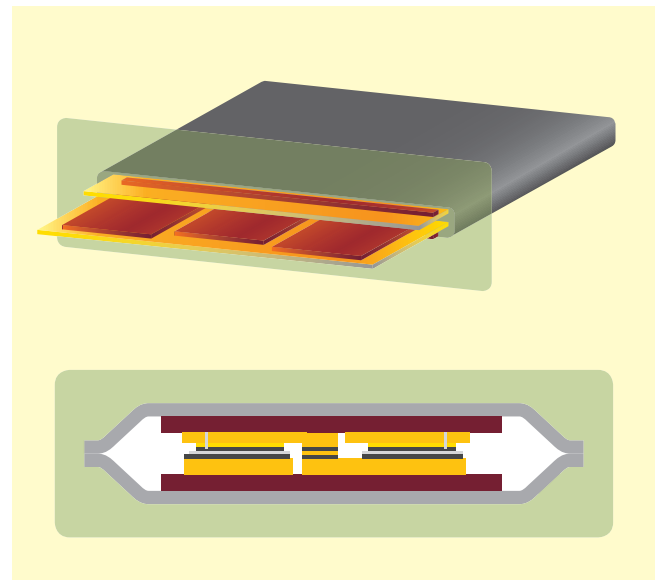


Figure 1: Schematic view and cross sectional view of a double sided cooled, double DBC assembly (“slot module”, Fraunhofer IISB), with semiconductor chips joined between the DBCs [1]

Model	R_{TH} K/W	$\frac{T_{MAX}}{T_{MEAN}}$	$\frac{T_{MIN}}{T_{MEAN}}$	ΔT relative
1. single sided cooling, bottom	0.691	1.23	0.82	0.41
2. single sided cooling, bottom (4-times)	0.349	1.32	0.73	0.59
3. single sided cooling, top, 22% centered	4.77	1.73	0.22	1.51
4. both sides cooling, top, entire area	0.341	1.24	0.81	0.43
5. both sides cooling, top, 19% centered	0.408	1.07	0.90	0.17
6. both sides cooling, top, 22% centered	0.401	1.06	0.93	0.13
7. both sides cooling, top, 25% centered	0.393	1.07	0.93	0.14
8. both sides cooling, top, 42% centered	0.365	1.15	0.92	0.23
9. both sides cooling, top, 46% connected, 22% centered not connected	0.356	1.46	0.85	0.61

Table 1: Results of the model calculation, thermal resistance R_{TH} , maximum and minimum chip temperature, each divided by the mean value by area of the chip temperature, as well as their difference

Model Calculations

Utilizing an axisymmetric approximation, the model describes the DBC – Si-chip – DBC stack, with 0.3/0.38/0.3 mm Cu-Al₂O₃-Cu DBCs, 0.2 mm thick Si and Ag sinter joints (30 μm). This sort of model has successfully been used before [2] with the advantage of short calculation times suitable for parameter variations. The lateral dimensions represent 10x 10 mm² Si, 15x 15 mm² Cu (DBC top side) and 25x 25 mm² DBC. Heat supply is performed by a constant power loss density in the upper 40 μm Si, the heat is removed to ambient temperature with a heat transfer coefficient of 5000 W m⁻² K⁻¹ acting at the DBC outer surface, which corresponds to a moderate water cooling. In figure 3 to 5, showing the temperature distribution within the stack, the temperature rise against ambient is shown. Mainly, the chip top contact area has been varied in size (percentage of chip area) and position.

Results

The results of the model calculations are presented in the table and graph. With good heat dissipation, there is always a temperature gradient from the chip center to the edge [3], due to lateral heat spreading in the substrate (figure 3). Indeed, the better the cooling, the wider is the temperature distribution on the chip, valid for single and both-sided cooling (table 1, model 1, 2 and 4, figure 2). The local junction temperature is known to affect reliability of conventional assemblies [4].

With the 4-fold heat transfer coefficient of 20 000 W m⁻² K⁻¹ acting at the DBC bottom side, which implies significantly improved flow conditions achieved by a more sophisticated cooling structure, one can achieve a thermal resistance with single-sided cooling being equal to double-sided cooling, however bought with a much higher temperature spread

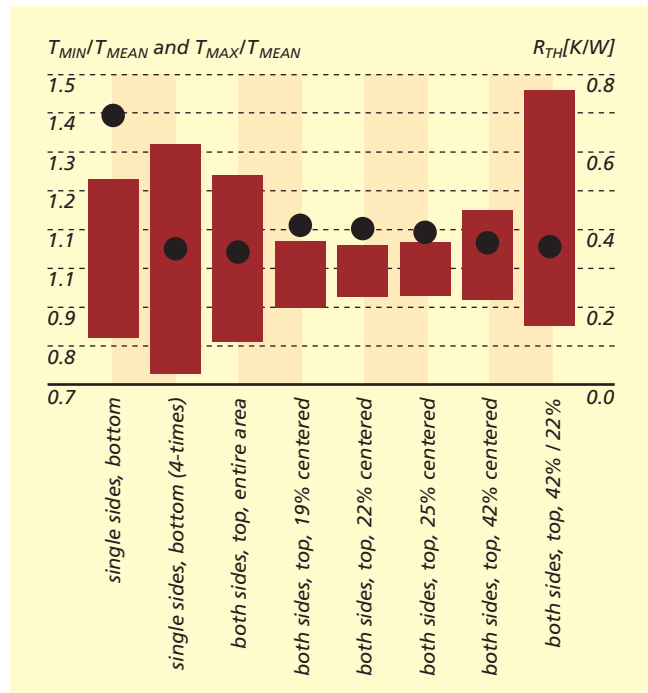


Figure 2: Results of the model calculations, spread of relative chip temperatures (columns) and thermal resistance R_{TH} (symbols)

on the chip (Table 1, Model 2). Thus, double-sided cooling appears to be efficient even with moderate effort in cooling channel design.

The non-relevant single-sided cooling via the partially joined top side (Table 1, Model 3) provides an unacceptable high thermal resistance together with an inadequate temperature spread (thus not included in figure 2).

The results further show, that the layout of the chip top contact can be used to effectively reduce the width of the temperature distribution (table 1, model 5 to 8, figure 4). Contacting the chip top side at an area less than 50% centrally favorably affects the width of the temperature distribution, with an optimum in terms of homogeneous chip temperatures at about 20 - 25% of the chip area at a slightly poorer thermal resistance. If the chip center is left out in the chip top side contact (Table 1, Model 9, Figure 5), i.e. the top contact compares to a ring shaped area on the chip surface, then the temperature distribution is considerably wider. In fact, in case of a temperature rise of 150 K at 25°C cooler temperature, the mean junction temperature of 175°C will be encountered, but locally a semiconductor temperature of 244°C will be caused by the temperature distribution, which is assumed to be functionally critical for Si semiconductors.

Discussion

As has been shown, the chip top side contact shape can be used as an efficient design parameter to optimize thermal performance in double-sided cooled assemblies. Since the heat source in the semiconductor is generally assumed closer to the Si chip-top side, the assembly is not strictly symmetric, i.e. the single sided cooling is even slightly worse than twice the thermal resistance of the double-sided cooling assembly when assumed ideal (table 1, model 1 and 4). The axisymmetric model overestimates the minimum chip temperatures, because the colder corners are not considered. Therefore, the width of the temperature distribution on the chip is larger, but uncritically extended to lower temperatures in reality. Experience has shown that the assessment of the critical high temperatures in the chip centre is largely mapped correctly. Although the discretization in the model is relatively coarse, with the grid lines shown in the graphs of the temperature distributions, the strong influence of the varied parameters is clearly visible.

Today, it is not yet fully understood, how the width of the temperature distribution on the chip affects its electrical performance. In addition to this thermal aspect, the electrical conductivity of the metallization is relevant in terms of current distribution [4], which in particular may result in the case of over-current to a local increase of the power loss and, thus, can cause a semiconductor defect. In almost all cases calculated here, the maximum DBC temperature on the cooler side is actually higher than the average chip temperature, and in the other cases only slightly lower. Thus, making use of the possible junction temperature, the water cooling circuit will convert locally to an evaporation cooler, a fact being less critical with regard to thermal resistance, but with regard to a corrosive attack (cavitation) or to a formation of deposits from possible contamination in the cooling medium [2]. Boiling can be counteracted with an increased pressure in the cooling circuit (for water about 5 bar for 150°C, nearly 10 bar for 175°C), while the common ethylene glycol admixture increases the boiling point by only a few degrees.

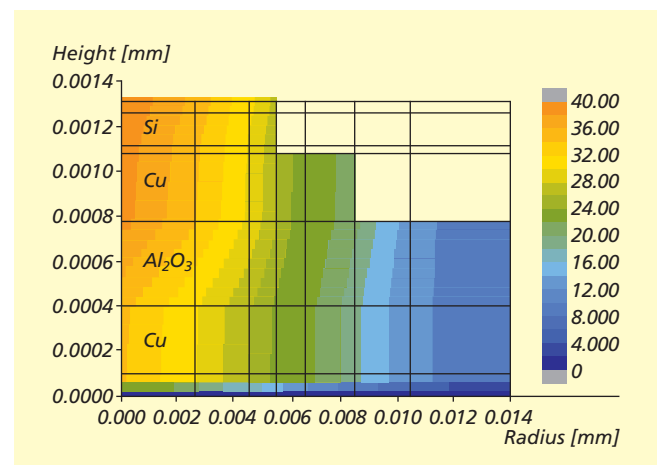


Figure 3: Temperature distribution within a conventional assembly Si-chip on DBC, single sided cooling, bottom, PL = 45 W (left = axis of symmetry at chip centre; right = DBC edge)

Conclusion, Summary

Of course, this parametric study is not intended to be exhaustive, but it already shows that top benefits can be achieved with double-sided cooling concepts, or significant disadvantages have to be taken into account, depending on the contact area on the chip top side.

With a centered top contact, a low thermal resistance combined with an almost homogeneous junction temperature can be achieved. Prerequisite for a favorable assembly concept is, of course, that the semiconductor manufacturer provides the chip layout and the metallization in such a manner that the gate contact is placed in a corner, and that the surface can be joined in a suitably large, centrally placed window.

For direct water cooling acting on the DBC, evaporative cooling is expected at higher loads, which has to be considered and optimized in terms of coolant medium and flow conditions.

References

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- [2] Max H. Poech, Modelling of Thermal Aspects of Power Electronic Assemblies, Proceedings IMAPS Nordic Annual Conference, Helsingør, Denmark, 26-28 September 2004, 120-125
- [3] Uwe Scheuermann, Ralf Schmidt, Investigations on the VCE(T)-Method to Determine the Junction Temperature by Using the Chip Itself as Sensor, PCIM Europe 2009, 802–807
- [4] Max H. Poech, Power Electronics Reliability – the Materials Behaviour is the Key, PCIM Europe 2010, 350–355 between the DBCs [1].

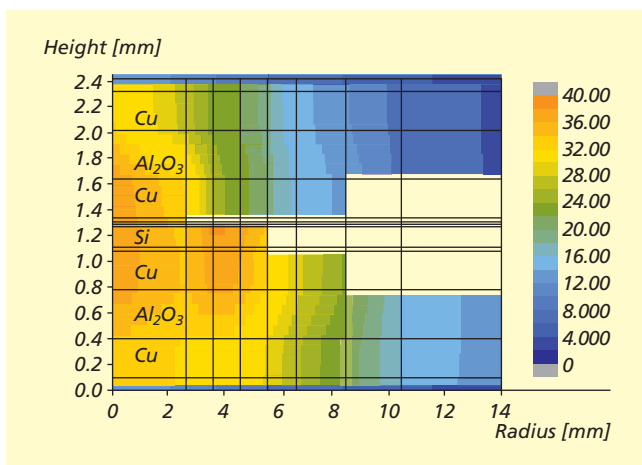


Figure 4: Temperature distribution within a double-sided cooled stack assembly DBC-Si-DBC, Si top contacted centrally at 22% of chip area, PL = 90 W

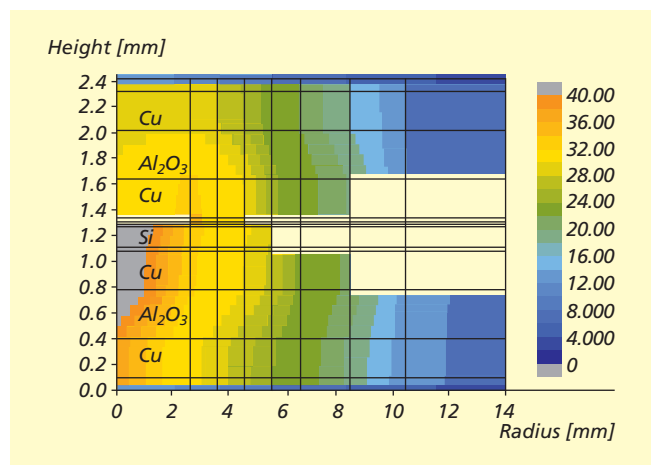


Figure 5: Temperature distribution within a double-sided cooled stack assembly DBC-Si-DBC, Si top contacted ring shaped with 46% of chip area, 22% centrally are not connected, PL = 90 W

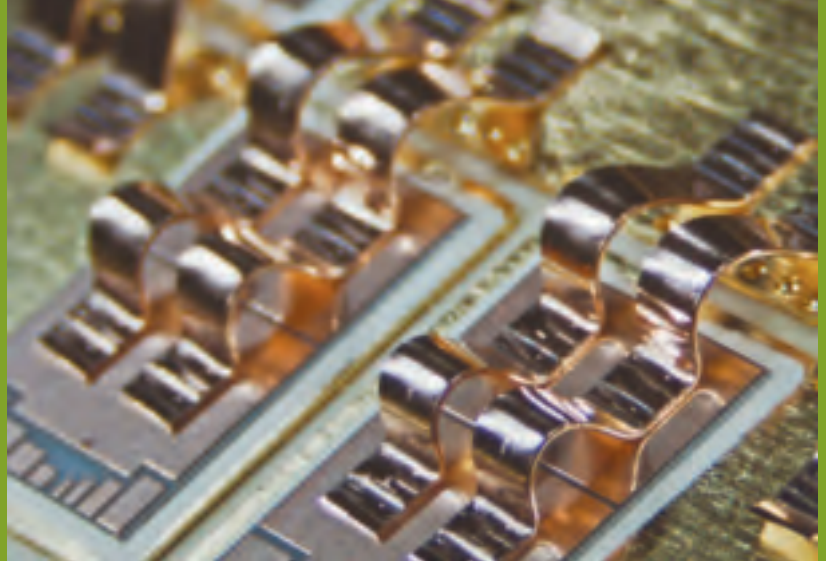


Figure 1: Copper ribbons connecting the top of the MAXIKON diode

COPPER RIBBON BONDING FOR POWER ELECTRONICS

High-power electronic modules define completely new requirements for innovative interconnection technologies: In a constant effort to reduce power losses, only an ultra-thin piece of silicon separates the current source and drain of, for example, an electronic power switch. Reliability is directly affected by heat generated due to ohmic resistance, but with increasingly pronounced voltage gradients required for higher switching voltage or frequencies, also parasitic capacitances play a major role. In off-state, the chip must withstand hundreds of volts potential difference with practically no leakage current that would impact the efficiency of the device.

In parallel to the continuously shrinking chip dimensions and rising reliability demands, power modules are heading for a production volume growth that will last many years.

Within the project MAXIKON, the Module Integration department at Fraunhofer ISIT focuses on the process development and characterization of a novel copper ribbon bonding technology, using ribbons of up to 2 mm width. A second research partner develops a pressure sinter technology for backside chip connections. The combination of both technologies should prevent the commonly seen degradation mechanisms in aluminum wire bonds and backside solder layers.

Copper ribbon bonding promises a reduction of wire bond interconnections in comparison to standard aluminum heavy wire bonding, thus the required chip geometry may be shrunk. The lower coefficient of thermal expansion (CTE) and the higher electrical and thermal conductivity of copper should reduce temperature induced defects of the welding interface to the chip electrode metallization. The very high mechanical strength of the ribbon is expected to generate robust substrate to power frame connections, with good tolerance to vibrations.

While these characteristics are very promising, a number of problems have to be solved in the process development: A standard heavy wire bonder is not able to provide enough bond force and ultrasonic power to form a weld. The wedge geometry has a large effect on the ultrasonic coupling into the ribbon. With standard aluminum ribbon wedges, a very short tool lifetime is observed. Cutting a 200 μm thick copper ribbon requires a special knife edge design and a powerful actuator behind. Loop forming demands a stiff wire guide that withstands high temperatures generated in ultrasonic welding. The copper ribbon is much harder than a standard aluminum chip metallization, hence the ribbon digs itself into the chip electrode, destroying the very sensitive transistor structures on the chip.

Fraunhofer ISIT has invested in a ribbon bonder BJ 939 of Hesse Mechatronics GmbH as a machine platform for developing copper ribbon bonding processes. The machine is equipped with three different bond heads to allow a fast tool change between aluminum and copper bonding, both as round wire and ribbons. A bond head change still necessitates recalibration of internal machine limits and welding parameter sets, which sums up to 30 minutes.



*Figure 2: Hesse Mechatronics
Bonder Bondjet 939*



*Figure 3: First staggered copper ribbon bonds
became possible with an advanced wedge design*

After first copper ribbon bonding trials on copper planes, ISIT's engineers quickly achieved successful bonds on DCB (direct copper bond) substrates and finally on chip surfaces. It hence became obvious that prismatic wedge geometries are not well suited to achieve industrial quality and tool lifetime expectations. The transition to a flat wedge geometry significantly increased tool lifetime and bond consistency, while avoiding plastic deformation of the chip's top metal layer. With this type of wedge design, 3D staggered ribbon bonds become possible that further increase the current flow capabilities in special applications.

Our studies quickly revealed a need for thicker chip metallization. Since a commercial power chip with an electroplated copper metallization was not available, ISIT developed the MAXIKON test diode as a vehicle for process development and active power cycling characterization. The test diode is very simple, but provides a junction temperature signal to control the power cycling. Power losses are generated just below the top chip surface to maximize the stress brought into the copper ribbon interface. The temperature calibration of sample diodes proved a very good homogeneity of the forward voltage at 50 mA constant current. This allows the use of the temperature calibration curve on all diodes without individual recalibration. The test diode is fabricated on 200 mm wafers, backgrinded to 150 μm and backside metalized for silver sintering. The front side contact metallization is electroplated copper on a titanium-copper plating base, with a thickness varied between 10, 25 and 40 μm . No underlying aluminum layer is present. Gate contacts with the same diode characteristics mimic different geometries found in IGBT chips to develop a high current capable interconnect by ultrasonic welded aluminum coated copper wire.

Functional samples have been built in different ribbon bond configurations based on a three-phase bridge circuit. Although the challenging power cycling tests ($\Delta T_j = 150 \text{ K}$) could not generate defects in the copper ribbon welding, limitations became visible in the DCB substrate and fracturing occurred in the interface between the die and the sintered silver backside layer.

The remaining project time will be dedicated to further investigations of these issues and the welding time will be reduced for a higher throughput.

The project MAXIKON is funded by the Federal Ministry of Economics and Technology under the Industrial Collective Research framework (IGF-17240) and supported by the German Federation of Industrial Research Associations (AiF).

REPRESENTATIVE RESULTS OF WORK

INTEGRATED POWER SYSTEMS

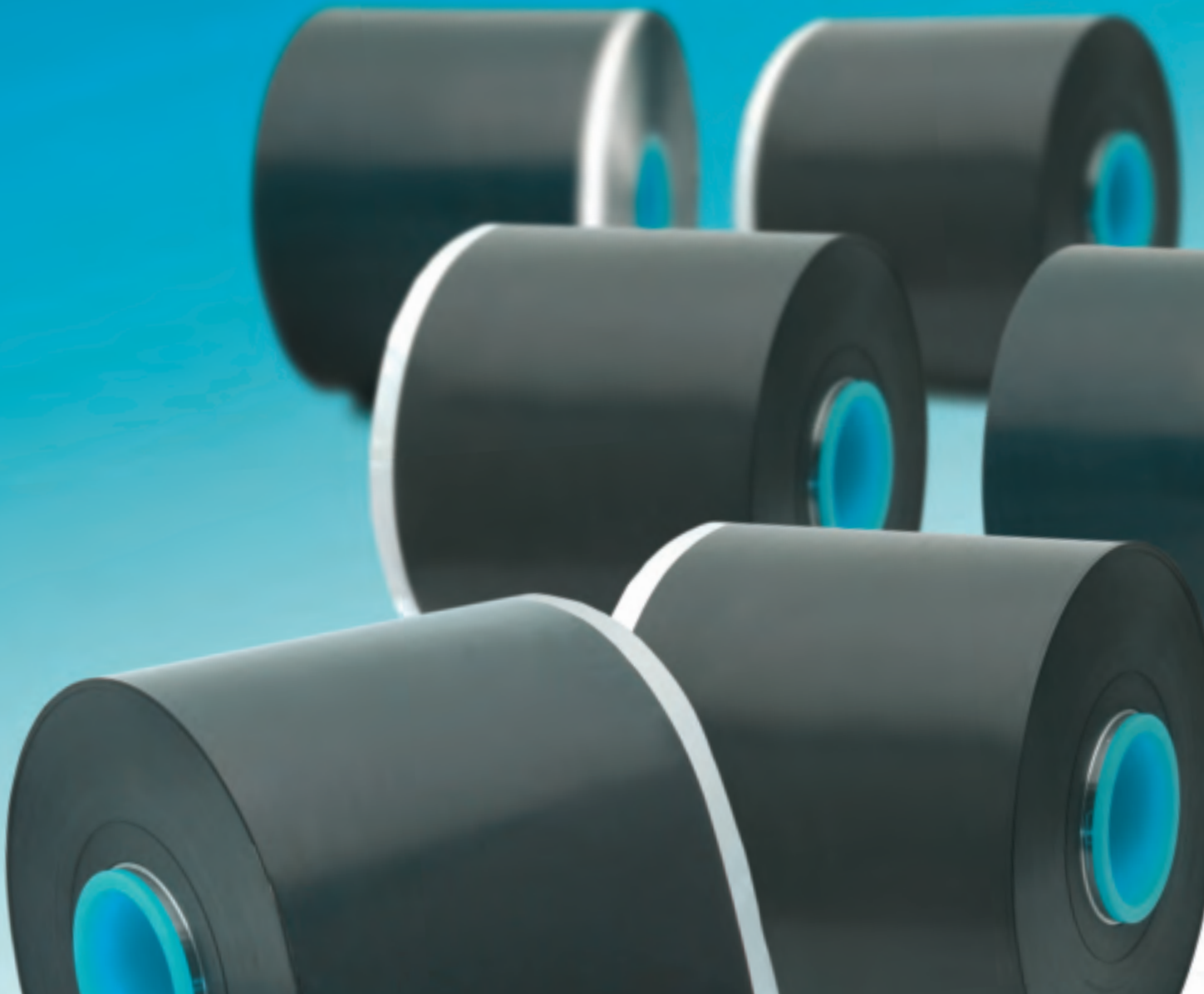




Figure 1: A single TIETeK cell provides a capacity of 20 Ah (width approx. 23 cm)



Figure 2: Pressure tolerant water sealed TIETeK battery module with 1 kWh capacity

PRESSURE TOLERANT BATTERY SYSTEM FOR DEEP SEA APPLICATIONS

Deep sea inspection and exploration tasks will play a crucial economic and scientific role in the future, leading to new market demands for robust surveying and monitoring vehicles at lower costs. Applications range from 3D water analysis to proximity pipeline inspection and high resolution mapping, like the exploration of manganese nodules.

Actual remotely and autonomous operated vehicles on the market are either large, heavy, and costly or insufficient. For this reason the Fraunhofer society has decided to develop advanced solutions for the most crucial components. Therefore several Fraunhofer institutes joined efforts on developing advanced components and realizing a demonstrator vehicle the TIETeK project.

Requirements and Solutions for TIETeK Deep Sea Battery Modules

Within this project, ISIT developed a modular battery system consisting of individual battery modules, which can be individually combined by the user to achieve the required capacity. Each module consists of 7 pairs of lithium polymer accumulator cells and a smart battery management system. All components have been designed and tested to withstand an ambient pressure of 600 bar which is equivalent to a water depth of 6000 m. Thus, no pressure vessel is required to protect cells and electronic. Instead a soft, transparent potting material has been used to seal them from the salt water.

Battery Cells – Requirements and Solutions

Besides the requirement of a very high pressure tolerance, the cells had to be optimized with respect to energy density and low temperature operation. To fulfill these requirements NCA has been used as cathode material in combination with graphite as anode, resulting in a usable cell voltage range between 3.0 V and 4.2 V. The separator was chosen from the

ISIT polymer separator family to ensure save operation and high pressure tolerance. Since hard case cells are not pressure tolerant a pouch case with an adapted geometry was selected (figure 1).

Finally, the electrolyte had to be optimized to fit the temperature requirements: The typical operating temperature during an underwater mission is in the range of 0°C to 4°C, whereas the storage temperature on board of the exploration vessel is similar to the air temperature, or even above during sun shine. After several tests in a climate chamber a standard electrolyte was chosen as compromise between storage temperature stability and operating temperature performance (figure 3).

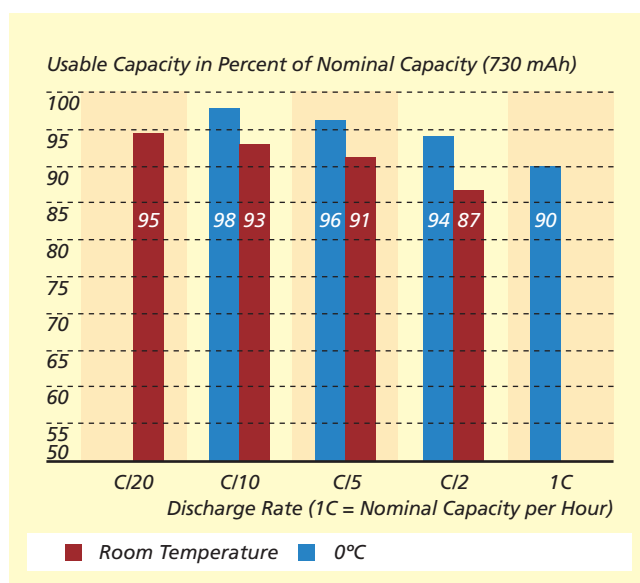


Figure 3: Discharge capacity of precursor cells at room temperature and 0°C

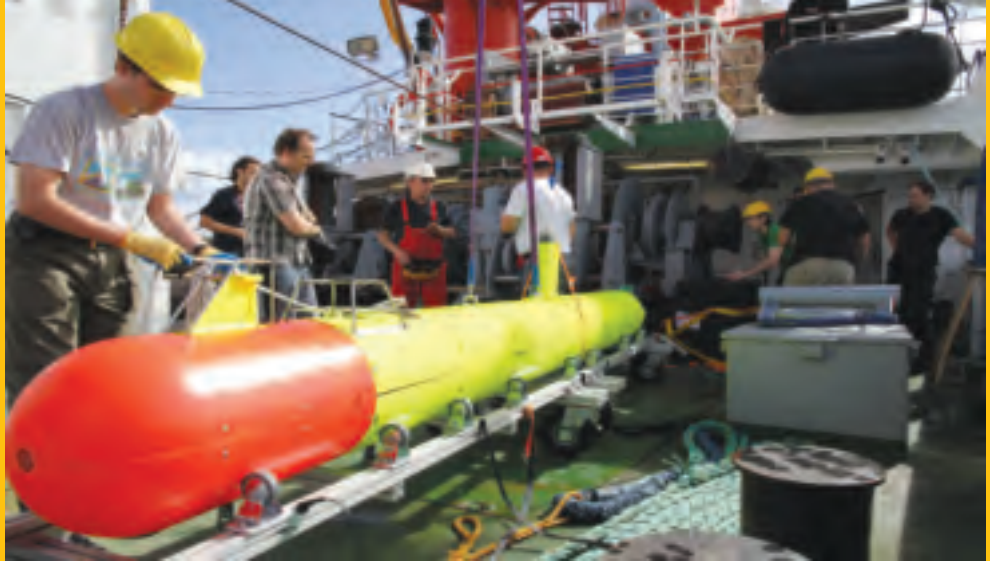


Figure 4: Autonomous underwater vehicle on board of a research ship (TIETeK)

The current linkage is figured out by using Nickel (for the anode) and Aluminum (for the cathode) connections. Usually, the interconnections between these electrodes are made by ultrasonic welding, laser welding, crimping or screwing. For this special application it was decided to solder the contacts, which is quite easy for the Nickel electrodes, but extremely difficult for Aluminum due to its very strong native oxide. Therefore, the outer parts of the Aluminum contacts have been plated with electroless Nickel Gold, resulting in a reliable and very good solderable surface.

In total, 133 cells were built and tested at 600 bar ambient pressure, with more than 90% performing correctly - a very good result since the cells are hand-crafted. Finally, one test module with 7 cells and 8 functional modules with 14 cells have been assembled. Thanks to continuous improvements of the manufacturing process, the following characteristics could be achieved:

- Self discharge rate: $\leq 2\text{mV} / \text{day}$ without pressure and $\leq 1\text{mV} / \text{h}$ at 600 bar
- Reversibility / cycle: 98.90 %
- Impedance: $6.2 \pm 1.6 \text{ mOhm} @ 1 \text{ kHz}$ and $6.7 \pm 1.8 \text{ mOhm} @ 100 \text{ mHz}$
- Cell capacity: $23 \pm 2.7 \text{ Ah}$ (figure 3)

Battery Management System

Save operation of lithium ion accumulators requires a battery management system that protects the cells from unhealthy or dangerous states and that balances all individual voltage levels within a narrow range.

Usually, the equalization is performed during the charge cycle, simply by bypassing current through a resistor. This method, called passive balancing, assures fully charged cells at the end of the charging. Unfortunately, the capacity of the cells is never equal. During discharge, the cell with the smallest capacity is the first one to get empty. As soon as this happens, the discharge has to be stopped to avoid an unhealthy or even dangerous deep discharge of this single cell. Thus, the weakest cell limits the capacity of the total battery module.

ISIT's battery management system with active cell balancing allows active charge transfer between cells at any time. During the charge cycle, active cell balancing reduces heat dissipation, which is essential for a watertight potted electronic system. During discharge, energy from strong cells is transferred to

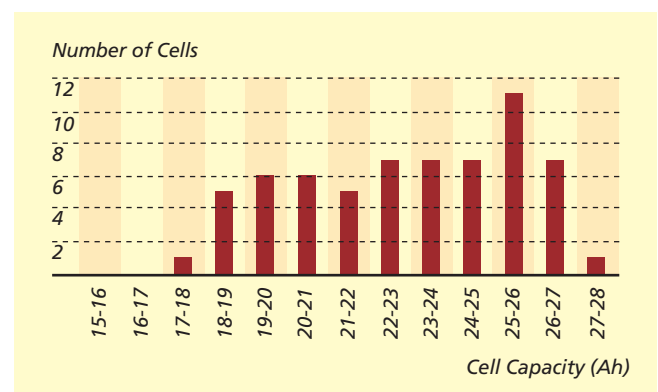


Figure 5: Distribution of cell capacities (Distribution of Cell Capacities (after Pressure Test))

weak ones, ensuring that all cells are empty at the same time. Thus, the full capacity of the battery module can be used.

In addition to the basic charge management features, the developed battery management system provides enhanced monitoring and remote control functionalities:

- Fail-safe protection against overvoltage is guaranteed by a redundant cell voltage measurement.
- A current sensor provides coulomb counting and short circuit protection.
- Integrated power switches enable protection against overcharge or deep discharge, as well as user controlled remote power switching.
- CANopen messaging communicates actual information like cell voltages, temperatures or state of charge (SOC).
- A light sensor can be triggered by a pocket torch to activate a SOC bar graph.
- Last but not least, a history logger stores all relevant measurement data and fault conditions.

The Final Battery Module

The final battery module can be seen in figure 2. The two heavy connectors are used for the power bus and the CANopen communication, the small connector is used for software updates and debugging issues. The reflective surface belongs to the flexible potting compound, which is totally transparent to enable visual user interaction with status LEDs and a light-sensor for activating the SOC bar graph with a pocket torch. Since the encapsulation must be void free, a vacuum potting process has been used. Good adhesion between compound and battery housing is ensured by combining a plasma activation process with a chemical adhesion promoter. The self-healing material allows the insertion of electrical probe tips for measurements without losing its watertight sealing properties.

Module Characteristics

Typical capacity: 41 Ah (1 kWh) at room temperature (reduced to 90% at 0°C)

Voltage range: 23,1 V to 29,7 V

Maximum current: 20 A

Total weight: 13,1 kg including module housing, metal inlay, underwater connectors and 3,5 kg potting material

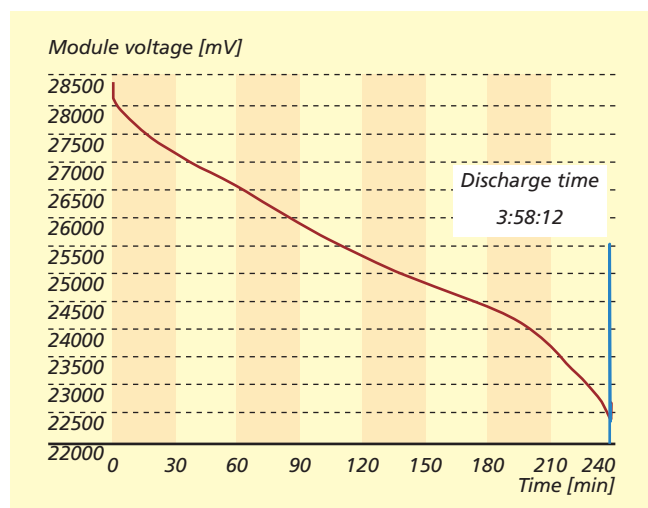


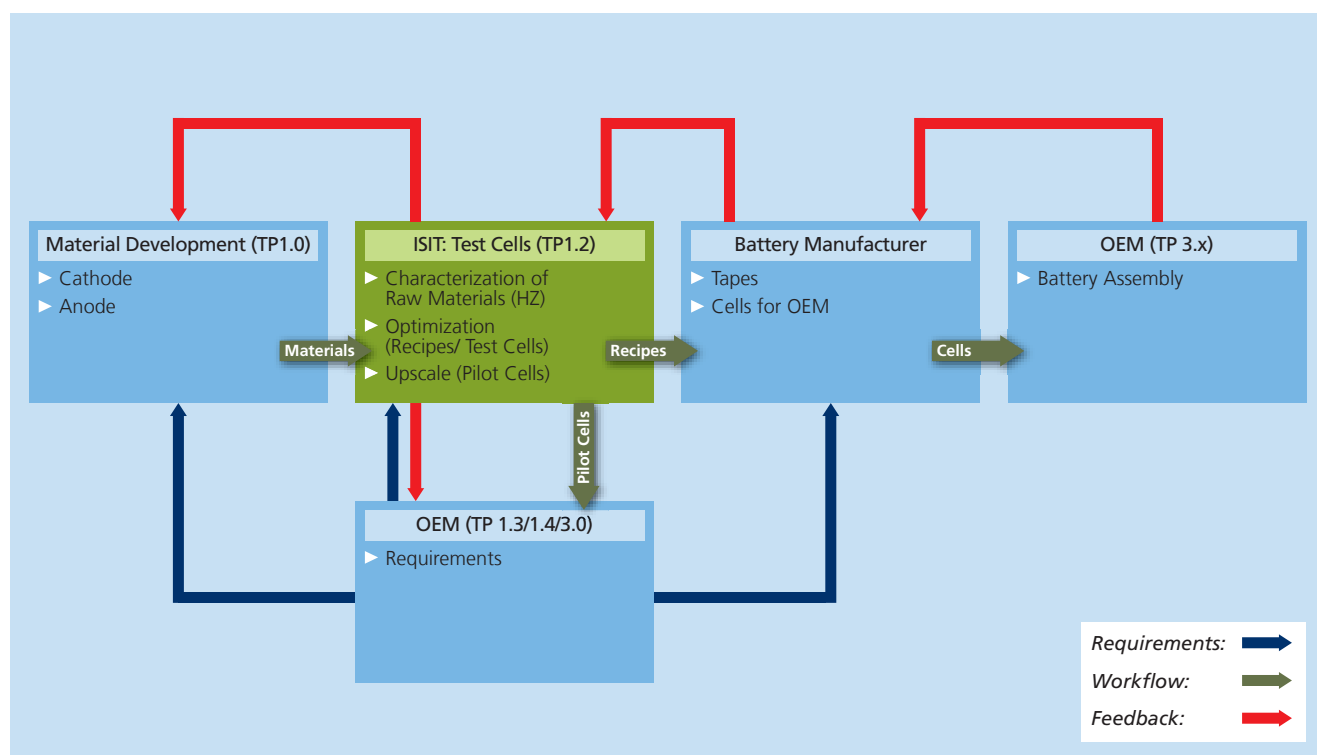
Figure 6: Discharge curve of the TIETeK module $c = 0,25$

LOW TEMPERATURE PERFORMANCE OF LITHIUM SECONDARY BATTERIES (PROJECT LINACORE)

Hybrid drive is one of the most promising options on the long and winding way to low-emission traffic. Safe, reliable and long lasting high power secondary batteries are one of the most challenging and critical key-elements of this technology. There is a huge demand for improvement at material-, cell- and systemlevel. Regarding hybrid electric vehicles (HEVs), German and European Automotive industries have to compensate some delay. But since a couple of years there has been a significant joint effort between industry and academic institutes to close this technological gap. Many projects addressing HEVs are supported by public funding from the German government.

The LINACORE project is embedded in a national research framework (Fünftes Energieforschungsprogramm der Bundesregierung) and addresses the complete value chain concerning the development, manufacturing and integration of secondary lithium ion batteries. The main objective of the project is the improvement of lithium battery technology with regard to the specific requirements of HEVs. The broad approach of the LINACORE-consortium covers all aspects related to battery manufacturing and integration.

Figure 1: Allocation of ISIT in the LINACORE project



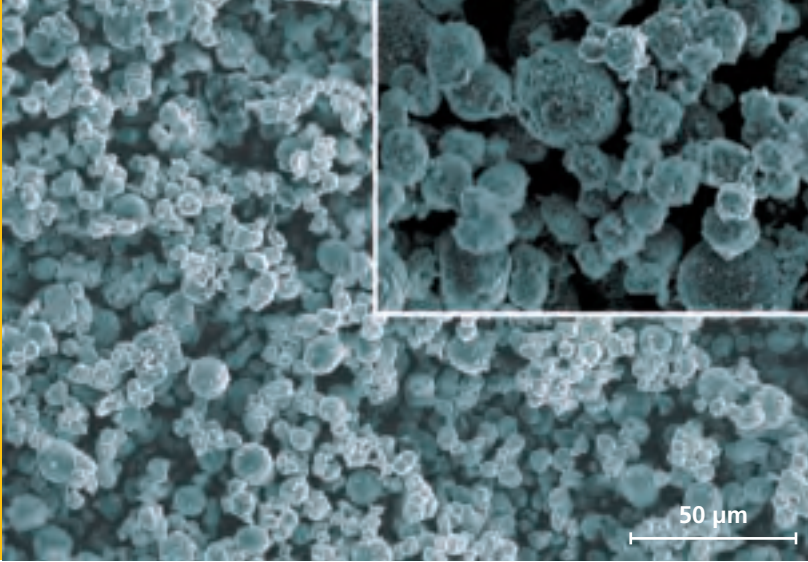


Figure 2: The morphology of a cathode material developed in the framework of LINACORE. The electrode material particles are comprised of smaller primary grains

Allocation of Fraunhofer ISIT

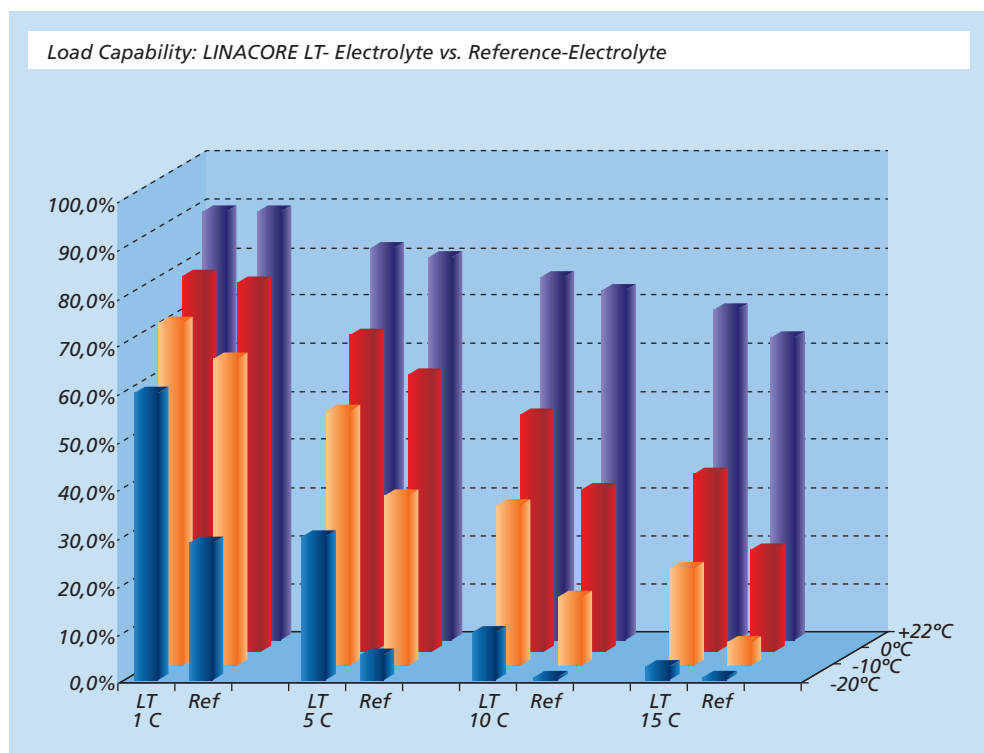
Fraunhofer ISIT acts as an interface between material suppliers, cell manufacturer and end users (figure .1). ISIT has characterized raw materials by different methods (e.g. half-cell measurements) and developed lithium polymer full-cells fitting the specific needs specified by a car manufacturer in the consortium. In a second step the electrode recipes have been transferred to the cell manufacturer. Besides safety, energy density and Total Cost of Ownership (TCO), the load capability of the battery plays a crucial role for HEVs. The ability for rapid charging (recuperation mode) and discharging (vehicle acceleration) processes even at a low system temperature is a critical aspect with still a lot of space for optimisation.

Here, at least three significant parameters are to be considered:

- a) particle size and morphology of the raw materials (material supplier)
- b) viscosity of solvent systems for electrolytes (material supplier)
- c) design of electrodes and cells (cell manufacturer)

The selection of suitable materials and a careful combination of the measures can result in a significant improvement of the low temperature performance without negative consequences for other requirement like safety, long term stability etc.

Figure 3: Discharge capacity (in half-cell-measurement) of a NCM-cathode material as a function of discharge current (c-rate) and temperature. The system with the low-temperature electrolyte (LT) shows a significant improvement in low temperature load capability compared to the reference electrolyte (Ref).



Results

In general a small particle size (nanoscale) and high specific surface area are prerequisites for a high load capability of an electrode material. This is due in part to short diffusion paths inside of the particles. To overcome processing problems caused by the particle size most of the material suppliers provide μm -sized agglomerates of nm-sized primary particles. Furthermore, this results in a reasonable load capability of the electrode material (figure 2).

- a) Electrolytes show a significant increase of cinematic viscosity with decreasing temperature. This unavoidable increase can be mitigated to a certain extent by a mixture of solvents with a suitable polarity and electrochemical stability. Low-temperature solvent blends may contain components with a low flash point. This has to be taken into consideration for the mandatory risk vs. benefit analysis.
- b) The overall performance of a cell is determined by the interaction of all the components of the system. In particular, the weakest link dominates the properties. To get reasonable results, all elements of the cell have to be optimised very carefully with regard to the low temperature performance (figure 4).

Summary

The joint effort of the LINACORE consortium in improving material properties and a careful optimization of the recipes and the cell design resulted in a remarkable improvement of the low temperature performance of the lithium polymer cells in comparison to the reference system tested in the beginning of the project.

Fraunhofer ISIT would like to thank all the partners in the LINACORE project. The project LINACORE has been funded by the Federal Ministry of Economics and Technology of Germany
Project partners: BASF AG, Robert Bosch GmbH, Volkswagen AG, SGL Carbon GmbH, Toda Kogyo Europe GmbH, Jacobs University Bremen GmbH, Westfälische Wilhelms-Universität Münster, Zentrum für Sonnenenergie- und Wasserstoff-Forschung Baden-Württemberg, Würth Solar GmbH & Co. KG.

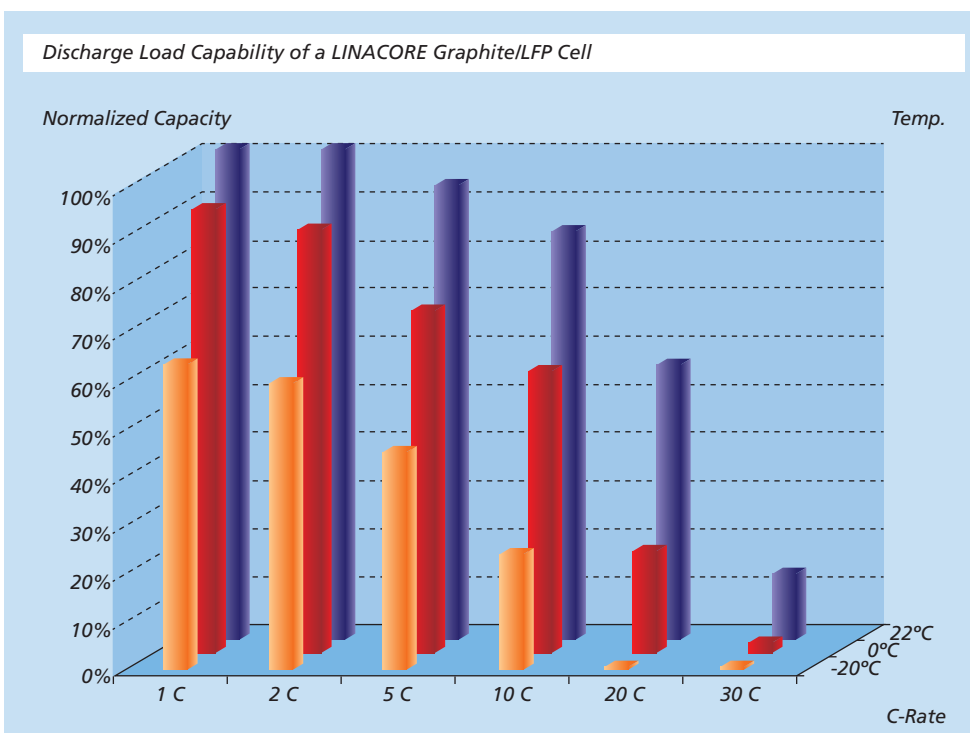


Figure 4: Discharge capability of an optimized low temperature cell consisting of LINACORE electrode materials and LINACORE electrolyte



IMPORTANT NAMES, DATA, EVENTS





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H. Schimanski

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Fachhochschule Lübeck

Westfälische Wilhelms-Universität, Münster

Sintef ICT, Oslo, Norway

École Polytechnique, Paris, France

University of Perugia, Italy

Universität Rostock

Süddänische Universität, Sonderburg, Denmark

VTT, Technical Research Center of Finland, Tampere, Finland

Politecnico di Torino, Italy

FBK, Trento, Italy

University of Twente, Netherlands

Fachhochschule Wedel

Institut für Polymertechnologien, Wismar



DISTINCTIONS

N. Lausen

Distinction of being best apprentice as „Mikrotechnologin - Mikrosystemtechnik“ at IHK Kiel for which she was awarded by the Fraunhofer-Gesellschaft, München, November 06, 2012

C. Mallas

Distinction of being best student at FameLab Germany, Lübeck, January 16, 2012

W. Reinert, M. Kontek, N. Lausen, R. Eisele, A. Hindel, F. Rudolf

*best poster award iPOWER², University of Warwick, Nov 2012
Process Development of Copper Ribbon High Current Interconnects*

V. Stenchly

*First Young Scientists, Best Poster Award for: Viscous Hot Glass Forming for Optical Wafer Level Packaging of Micro Mirrors
The 26th European Conference on Solid-State Transducers: Eurosensors 2012, 9-12. September, Krakau, Polen.*

TRADE FAIRS AND EXHIBITIONS

BATTERY JAPAN 2012

3rd International Rechargeable Battery Expo, in cooperation with Fraunhofer Netzwerk Batterien, February 29 – March 02, 2012, Tokio, Japan

Energy Storage 2012

March 13 – 14, 2012, Düsseldorf

New Energy 2012

March 15 – 18, 2012, Husum

Anuga FoodTec 2012

*The International Trade Fair for Food and Drink Technology
March 27 – 30, 2012, Köln*

Analytica 2012

*23rd Internationale Trade Fair for Laboratory Technology, Analysis, Biotechnology and Analytica Conference
April 17 – 20, 2012, München*

SMT 2012

Hybrid Packaging System Integration in Micro Electronics, May 8 – 10, 2012, Nürnberg

Control 2012

International Trade Fair for Quality Assurance, May 8 – 10, 2012, Stuttgart

PCIM 2012

International Exhibition & Conference, Power Conversion Intelligent Motion, May 08 – 10, 2012, Nürnberg

TechConnect World 2012

June 18 – 21, 2012, Santa Clara, CA

MedTech Pharma 2012

July 4 – 5, 2012 Nürnberg

Micromachine/MEMS 2012

July 11 – 13, 2012, Tokio, Japan

FED Conference 2012

September 20 – 22, 2012, Dresden

AZUBIZ 2012

Regional Training Fair, September 28, 2012, Regionales Berufsbildungszentrum, Itzehoe

ISIT Exhibition at Thalia Bookstore Hamburg,

October 22 – November 19, 2012, Hamburg

Jobaktiv Metropolregion Hamburg 2012

Akademiker im Norden, November 6, 2012, CCH, Hamburg

BIO Europe 2012

November 12 – 14, 2012, Hamburg

Electronica 2012

25th International Trade Fair for Electronic Components Systems and Applications, November 13 – 16, 2012, München

MISCELLANEOUS
EVENTS

Aspekte moderner Silizium-technologie

Public lectures, monthly presentations, Fraunhofer ISIT, Itzehoe

Praxisorientierte Prozess-optimierung in der elektronischen Baugruppenfertigung

Seminar: February 07 – 11, December 05 – 09, 2012, Fraunhofer ISIT, Itzehoe

ISIT Presentation in framework of „Macht mit bei Mint – Zukunftsberufe für Frauen“

Information day for school-girls, initiated by Volkshochschulen Kreis Steinburg, February 14, 2012, Fraunhofer ISIT, Itzehoe

Der optimierte Rework-Prozess

Lernen Sie Ihren Reparaturprozess sicher zu beherrschen. Seminar: Feb. 29 – March 02 and November 28 – 30, 2012, Fraunhofer ISIT, Itzehoe

Manuelles Handlöten in Theorie und Praxis

Training within the Project QMIT (Qualifizierungsinitiative Mikrotechnologie), Qualifizierungsmodul 4, March 6, 2012, Fraunhofer ISIT, Itzehoe

Lotpastenapplikation

Technologien, Prozessoptimierung, ehlervermeidung Seminar: March 12 – 13 and November 5 – 6, 2012, Fraunhofer ISIT, Itzehoe

Temperaturmesstechnik

Temperaturmessung richtig durchgeführt, Seminar: March 14 and Nov. 07, 2012, Fraunhofer ISIT, Itzehoe

Reflowprofiloptimierung

Vom Wärmefluss in der Lötanlage zum optimierten Lötprofil, Seminar: March 15 and November 8, 2012, Fraunhofer ISIT, Itzehoe

Information visit of H. Rickers, member of state parliament together with regional economic politicians at ISIT, Speakers: D. Austermann, member of ISIT advisory board

Prof. R.Thiericke, director of the innovation center Itzehoe, Prof. W. Benecke, ISIT managing director, H. Rickers MdL, April 13, 2012 Fraunhofer ISIT, Itzehoe

Technologietrends in der Baugruppenfertigung

Technologietag im Fraunhofer ISIT, Seminar: April 18, 2012, Fraunhofer ISIT, Itzehoe

Die beherrschbare Baugruppenfertigung

Herstellungsqualität, Fehleranalyse und Prozessoptimierung, Seminar: April 24 – 26 and Sept. 25 – 27, 2012, Fraunhofer ISIT, Itzehoe

Optimierung von Selektiv- und Wellenlötprozessen

Training within the Project QMIT (Qualifizierungsinitiative Mikrotechnologie), Qualifizierungsmodul 10, May 22, 2012, Fraunhofer ISIT, Itzehoe

Optimierung von Lötprozessen

Training within the Project QMIT, Qualifizierungsmodul 13, August 21 – 22, 2012, Fraunhofer ISIT, Itzehoe

Manuelles Handlöten in Theorie und Praxis

Training within the Project QMIT, Qualifizierungsmodul 17, August 15, 2012, Fraunhofer ISIT, Itzehoe

Inspektionsverfahren und Fehleranalyse zur Baugruppenbewertung

Training within the Project QMIT, Qualifizierungsmodul 15, September 17 – 18, 2012, Fraunhofer ISIT, Itzehoe

microtech nord

3. Norddeutscher Mikroelektronik-Tag, „Energiewende mit Effizienz – Herausforderung für die Mikrotechnologie“, September 20, 2011 Fraunhofer ISIT, Itzehoe

Information visit at ISIT of R. Meyer, minister of economy, labour, transport and technology of Schleswig-Holstein

Speakers: Prof. U. Buller, senior vice president of Fraunhofer-Gesellschaft, Prof. W. Benecke, ISIT managing director, R. Meyer, minister of economic affairs, Oct. 2, 2012, Fraunhofer ISIT, Itzehoe

Der optimierte Rework-Prozess

Training within the Project QMIT, Qualifizierungsmodul 16, October 30, 2012, Fraunhofer ISIT, Itzehoe

Herausforderungen durch ESD (Electro-Static-Discharge)

Training within the Project QMIT, Qualifizierungsmodul 18, November 11, 2012, Fraunhofer ISIT, Itzehoe

Roofing ceremony of the new ISIT cleanroom building

Speakers: R. Müller-Beck, state secretary at ministry of economics, Kiel, Prof. A. Gossner, senior vice president of the Fraunhofer-Gesellschaft, Prof. W. Benecke, ISIT managing director, Dr. A. Köppen, mayor of the city Itzehoe, November 23, 2012, Fraunhofer ISIT, Itzehoe

Wellenlötten und Selektivlötten

Technologien, Fehlervermeidung durch Prozessoptimierung, Qualitätsbewertung, Seminar: Dec. 11 – 12, 2012, Fraunhofer ISIT, Itzehoe

Praktische Metallographie und Interpretation von Schlifffproben

Training within the Project QMIT, Qualifizierungsmodul 20, Dec. 17–18, 2012, Fraunhofer ISIT, Itzehoe



JOURNAL PAPERS, PUBLICATIONS AND CONTRIBUTIONS TO CONFERENCES

L. Blohm, E. Nebling, G. Melmer

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U. Hofmann, M. Aikio

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M. Poech
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Micro-Cantilevers with AlN Actuators and PtSi Tips for Multi-Frequency Atomic Force Microscopy. Review of Scientific Instruments 83, 096107, September, 2012

J. Rudzki, L. Jensen, M. Poech, L. Schmidt, F. Osterwald
Quality Evaluation and Process Control for Silver Sintering Layers in Power Electronic modules.
 CIPS 2012 Nuremberg, paper P 24, pp. 231–236, March, 6 – 8, 2012

H. Schimanski
Sichere manuelle Lötprozesse an bleifreien elektronischen Baugruppen.
 Konferenzband EBL 2012, p.175–180; Fellbach, February 14 – 15, 2012

H. Schimanski
Optimierte Reworkprozesse an komplexen Baugruppen.
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H. Schimanski
Reflowprofiloptimierung.
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C. Schröder, F. Senger, F. Stoppel, B. Wagner, W. Benecke
Wafer-Level Packaging of AlN-based Piezoelectric Micropower Generators Poster.
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B. Steible, M. Stoldt, M. Tack, G. Zwicker
Application of an Abrasive-Free Cu Slurry for MEMS Devices
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TALKS AND POSTER PRESENTATIONS

L. Blohm, F. Altenbernd, J. Albers, G. Piechotta, S. Holz, E. Nebling

pH-Measurement with Iridium-Electrodes. Statusseminar Fraunhofer-Systemforschung „Zellfreie Bioproduktion“, Berlin, March 15-16, 2012

R. Dudde

Optimised Piezoelectric PZT Thin Film Production on 8" Silicon Wafers for Micro-mechanical Applications. Nanotech 2012, Santa Clara, CA, 2012, June 18-21, 2012

R. Dudde

Production of Advanced MEMS Devices, MEMS Foundry Itzehoe. Micromachine/MEMS 2012, Tokio, Japan. July 11-13, 2012

J. Eichholz

Dynamischer Operationsverstärker mit geringem Ruhestrom für Anwendungen in der Mikrosystemtechnik. Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, September 05, 2012

D. Friedrich

Fortschrittliche Halbleitertechnologien für energieeffiziente Si-Leistungsbaulemente. Seminar Elektromobilität der CCG (Carl-Cranz Gesellschaft e.V.) organized by Helmut-Schmidt Universität, Hamburg, September 17–19, 2012

U. Hofmann

Biaxial tripod MEMS Mirror for Low-Cost Laserscanners. MiniFaros-Final Event, Hamburg, December 13, 2012

H. Kapels

Realisierung eines bidirektionalen DC/DC-Wandlers für Photovoltaikanlagen mit Zwischenspeicher. Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, November 07, 2012

T. Knieling

Gedruckte Elektronik: Funktionelle Elemente aus Low-Invest-Verfahren. Technologietag ISIT, Itzehoe, April 18, 2012

T. Knieling

Inspektionsverfahren für Elektronikkomponenten und -systeme. QMIT-Seminar IZET, Itzehoe, September 17, 2012

T. Knieling

Use of Combination 2D and CT Scan X-Ray Imaging for Solder Joint Inspection. 8. Symposium General Electric, Ahrensburg, October 16, 2012

T. Knieling, N. Marengo

Hybride Elektronik: Flexible Systeme auf Papier und Plastik. Chemitzer Seminare, Chemitz, December 11, 2012

K. Kohlmann, R. Dudde, D. Friedrich

Competence Center for Power Electronics, Schleswig-Holstein. Development of an Advanced, Modular Frequency Converter for Traction Control. Smart Systems Integration Conference, Zürich, March 21-22, 2012

J. Lähn

Temperaturmessung richtig durchgeführt. ISIT-Seminar: Temperaturmesstechnik, Itzehoe, March 14, 2012

S. Marauska

Magnetoelektrische Sensoren für biomedizinische Anwendungen. Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, May 02, 2012

E. Nebling

BMBF-Projekt: Zellfreie Bioproduktion. Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, February 01, 2012

E. Nebling

POC-Diagnostik mittels siliziumbasierter Chiptechnologie. 3. Kongress „MedTech Pharma 2012“, Session „Diagnostics, NCC Ost Nürnberg Messe, July 04-05, 2012

E. Nebling

Biologie und Silizium - unmöglich? 6. Science Summer School Itzehoe, IZET Itzehoe, August 13–17, 2012

E. Nebling

Silizium und Biologie? Gastvortrag am Gymnasium Dörpsweg, Hamburg, November 29, 2012

G. Piechotta

Mobile Analyseplattform für die Vor-Ort-Detektion von Inhaltsstoffen und Qualitätsparametern – vom Futter bis zur Milch. 7. Ideenbörse Forschung vom Milchindustrieverband, Fulda, November 14-15, 2012

M. H. Poech

1) Werkstoffe der Aufbau- und Verbindungstechnik (AVT). 2) Werkstoffe der AVT (II). 3) Passive Bauelemente, Schaltungsträger, Kühlkörper. 4) AVT für Systeme kleiner und mittlerer Leistung. 5) Fehlermechanismen. ECPE Cluster – Schulung „Aufbau- und Verbindungstechnik (AVT) in der Leistungselektronik“, Hanau, March 28-29, 2012,

M. H. Poech

Temperaturmessung im Reflow – Was gilt es zu beachten? ISIT Seminar: Temperaturmesstechnik, Itzehoe, March 14, 2012 and November 07, 2012

**M. H. Poech**

Das Reflow-Lötprofil bei eingeschränktem Prozessfenster.
ISIT-Seminar: Die beherrschbare Baugruppenfertigung, Itzehoe, April 24 – 26, 2012 and September 25 – 27, 2012

M. H. Poech

Selektivlöten in der Leistungselektronik.
ISIT-Seminar: Die beherrschbare Baugruppenfertigung, Itzehoe, April 24 – 26, 2012 and September 25 – 27, 2012

M. H. Poech

In-situ-Untersuchungen zur Porenentstehung.
4. Berliner Technologieforum „Voids in Lötstellen“, Siemens CT, Berlin, May 31, 2012

M. H. Poech

Löten von Hochstromleiterplatten.
Industriearbeitskreis „Produktionstechnik in der Leistungselektronik“, Leiterplattentechnik für die Leistungselektronik, Schweizer Electronic AG, Schramberg, June, 26, 2012

M. H. Poech

High Current Printed Circuit Boards (PCBs) and Suitable Connection Techniques.
ECPE Workshop „Integrated Power Boards“, Delf, November 21-22, 2012,

M. H. Poech

Zuverlässigkeit von Baugruppen.
ISIT-Seminar: Die beherrschbare Baugruppenfertigung, Itzehoe, April 24 – 26, 2012 and September 25 – 27, 2012

W. Reinert, V. Stenchly, C. Roman, S. Cortial

Toolbox Development for Uncooled FIR μ -Bolometer Image Sensors. EPTC 2012, Singapore December, 2012

M. Reiter

Baugruppen- und Fehlerbewertung.
ISIT-Seminar: Die beherrschbare Baugruppenfertigung, Itzehoe, April 24-26, 2012 and September 25-27, 2012

H. Schimanski

Reflowprofiloptimierung auf Basis bestehender Standards.
FED-RG HH & Hamburger Lötzirkel auf der Nortec, Hamburg, January 25, 2012

H. Schimanski

Sichere manuelle Lötprozesse an bleifreien elektronischen Baugruppen.
EBL 2012; Fellbach, February 14-15, 2012

H. Schimanski

Prozessfehler und ihre Auswirkungen.
Juki-Technologietag – Juki meets friends Itzehoe, February 23, 2012

H. Schimanski

Der optimierte Rework-Prozess.
QMIT-Seminar: Der optimierte Rework-Prozess, February 29-March 02, 2012, ISIT, Itzehoe and October 30, 2012

H. Schimanski

(Bleifrei) Reparaturlöten.
ISIT-Seminar: Der optimierte Rework-Prozess, Itzehoe, February 29 – March 02, 2012 and November 28-30, 2012 and QMIT-Seminar: Manuelles Löten von SMD- und THT-Bauelementen auch mit bleifreien Loten, ISIT, Itzehoe, March 05, 2012

H. Schimanski

Baugruppen schonende Reparatur komplexer SMT-Baugruppen.
ISIT-Seminar: Der optimierte Rework-Prozess, Itzehoe, February 29 – March 02, 2012 and November 28-30, 2012

H. Schimanski

Baugruppen- und Fehlerbewertung, ISIT-Seminar: Der optimierte Rework-Prozess, Itzehoe, February 29 – March 02, 2012 and November 28-30, 2012 and QMIT-Seminar: Manuelles Löten von SMD- und THT-Bauelementen auch mit bleifreien Loten, Itzehoe, March 05, 2012

H. Schimanski

Bleifrei Handlöten.
QMIT-Seminar: Manuelles Löten von SMD- und THT-Bauelementen auch mit bleifreien Loten, ISIT, Itzehoe, March 05, 2012 and August 15, 2012

H. Schimanski

Lotpastenauftrag durch Jetprinten und Lotpasteninspektion. ISIT-Seminar: Lotpastenapplikation, Itzehoe, March 12 – 13, 2012

H. Schimanski

Temperaturmessung richtig durchgeführt.
ISIT-Seminar: Temperaturmesstechnik, Itzehoe, March 14, 2012 and November 07, 2012 and QMIT-Seminar: Temperaturmesstechnik, ISIT, Itzehoe, August 21, 2012

H. Schimanski

Der Reflow-Lötprozess
ISIT-Seminar: Reflowprofiloptimierung, Itzehoe, March 15, 2012 and November 08, 2012 and QMIT-Seminar: Reflowprofiloptimierung, ISIT, Itzehoe, August 22, 2012

H. Schimanski

Technologietrends in der Baugruppenfertigung.
Technologietag, Itzehoe, April 18, 2012

TALKS AND POSTER PRESENTATIONS

H. Schimanski

Lötqualität und Reflow-Lötverfahren. ISIT-Seminar: Die beherrschbare Baugruppenfertigung, Itzehoe, April 24–26, 2012

H. Schimanski

Qualitätsprüfung an Leiterplatten. ISIT-Seminar: Die beherrschbare Baugruppenfertigung, Itzehoe, April 24–26, 2012

H. Schimanski

Prozessfenster und Zuverlässigkeit manuell reparierter Lötstellen. ISIT-Seminar: Die beherrschbare Baugruppenfertigung, Itzehoe, April 24–26, 2012

H. Schimanski

Optimierte Reworkprozesse. AK „Zuverlässige bleifreie Systeme“, Nürnberg, May 07, 2012

H. Schimanski

Qualitätsbewertung in Anlehnung an IPC-Standards. QMIT-Seminar: Inspektionsverfahren und Fehleranalyse zur Baugruppenbewertung, ISIT, Itzehoe, September 17 – 18, 2012

H. Schimanski

Optimierte Reworkprozesse an komplexen Baugruppen. 20. FED-Konferenz, Dresden, September 20 – 22, 2012

H. Schimanski

Reflowprofiloptimierung. 20. FED-Konferenz, Dresden, September 20–22, 2012

H. Schimanski

Lötqualität und Reflow-Lötverfahren. ISIT-Seminar: Die beherrschbare Baugruppenfertigung, Itzehoe, September 25–27, 2012

H. Schimanski

Einflussfaktoren im Lotpastendruck. ISIT-Seminar: Die beherrschbare Baugruppenfertigung, Itzehoe, September 25–27, 2012

H. Schimanski

Prozessfenster und Zuverlässigkeit manuell reparierter Lötstellen. ISIT-Seminar: Die beherrschbare Baugruppenfertigung, Itzehoe, September 25–27, 2012

H. Schimanski

Einflussfaktoren im Lotpastendruck. ISIT-Seminar: Lotpastenapplikation, Itzehoe, November 05–06, 2012

H. Schimanski

Jetprinten und Lotpasteninspektion. ISIT-Seminar: Lotpastenapplikation, Itzehoe, November 05–06, 2012

H. Schimanski

Lötprofiloptimierung und Qualitätsbewertung. ISIT-Seminar: Wellenlöten und Selektivlöten, ISIT, Itzehoe, December 11–12, 2012

C. Schröder, F. Senger,

F. Stoppel, B. Wagner,

W. Benecke

Wafer-Level Packaging of AlN-based Piezoelectric Micropower Generators. PowerMEMS 2012, Atlanta, USA, December 3, 2012

O. Schwarzelbach

Produktionsnahe Messtechnik auf Waferebene für MEMS. Aspekte moderner Siliziumtechnologie, von Glaswafern. Fraunhofer ISIT, Itzehoe, April 04, 2012

V. Stenchly

Heißformgebung von Glaswafern für den Aufbau mikrooptischer Bauelemente. Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, October 10, 2012

A. Würsig

Stationäre Energiespeicher für Home-Solar-Anlagen – Entwicklung und Potentiale. Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, June 06, 2012

H. Züge

Hochvolt PowerMOS – Neue Kompensationsbauelemente nach dem Super Junction Prinzip. Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, December 05, 2012

DIPLOMA, MASTER'S AND BACHELOR'S THESES

Shaghayegh Arab

Entwicklung eines Gesamtprozesses zum Thermokompressionsbonden und Evaluierung verschiedener Hermetizitätsprüfverfahren zur Herstellung vakuumverkapselter Mikrogehäuse. Diploma theses, FH Lübeck, December, 2012

Yannick Bockholt

Entwicklung eines energiesparenden Energie-Management-Systems mit präziser Strom- und Spannungsmessung. Bachelor's theses, FH Wedel, September, 2012

Jan-Eric Lange

Charakterisierung magnetischer Eigenschaften eines ferro-magnetischen Bauelements auf Si-Wafer-Ebene. Master's theses, FH Westküste, November 2, 2012

Michael Kampmann

Entwicklung piezoelektrischer Mikroaktuatoren für aktive optische Bauelemente. Diploma theses, University of Bremen, September, 2012

Jan Labahn

Programmierung von Messroutinen zur Charakterisierung von Leistungstransistoren für Serienmessung auf einem Wafer-Prober unter Einbindung eines Thermochucks. Bachelor's theses, FH Lübeck, Januar, 2012

Christian Mallas

Realisierung einer adaptiven Regelung eines mikromechanischen Spiegels mit Hilfe eines FPGA-basierten DSP-Systems. Diploma theses, CAU Kiel, August 20, 2012

Inga Medina-Diaz

Evaluierung des Messverfahrens „Single Electrode Redox Cycling“ für Immunoassays auf elektrischen Multipositions-Biochips. Bachelor's theses, HAW, August, 2012

Michael Pleßen

Entwurf eines differenziellen Operationsverstärkers in einer 0,35µm-CMOS-Technologie. Master's theses, FH Westküste, January, 2012

Felix Christoph Schröder

Untersuchung der statischen und dynamischen elektrischen Eigenschaften von High Voltage Fast Recovery Dioden. Bachelor' theses, FH Kiel, August, 2012

Saskia Schröder

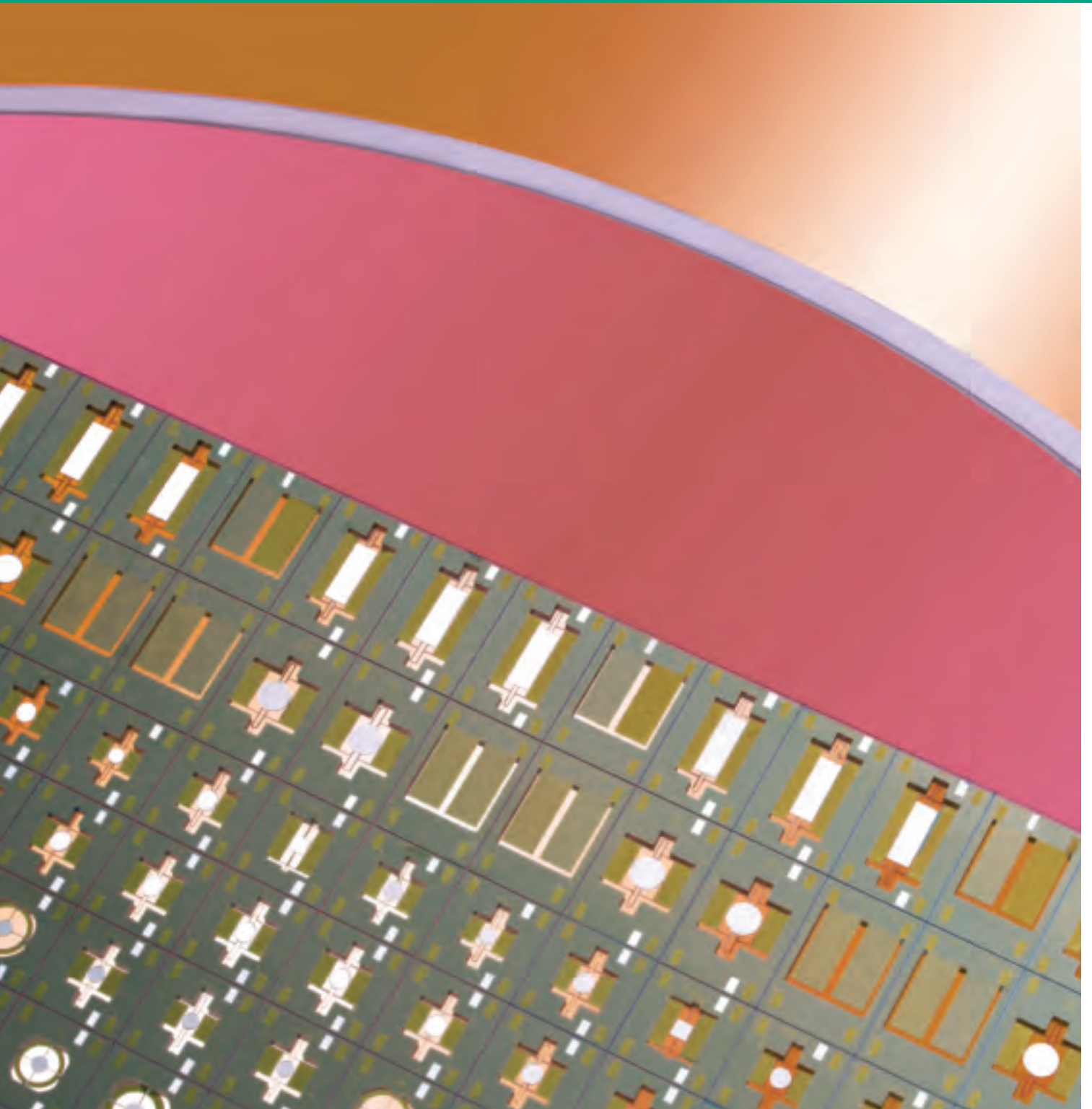
Qualifizierung eines Heißgas Reparatur-Lötprozesses. Bachelor's theses, FH Westküste, February 01, 2012

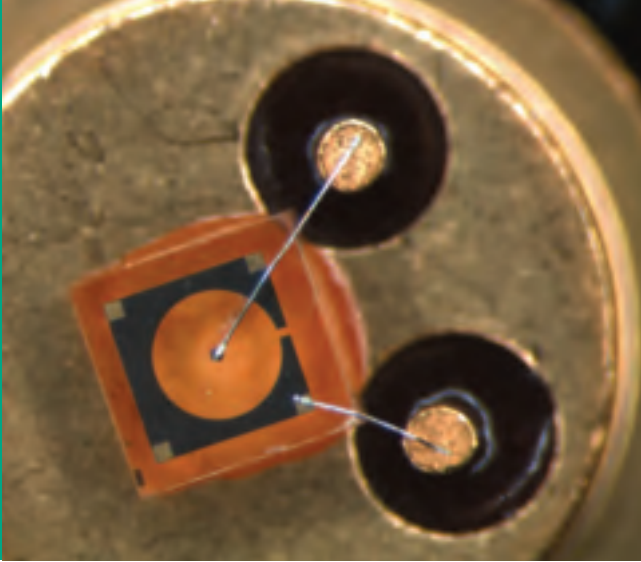
Hanno Sternberg

Konzipierung, Implementierung und Validierung eines Batterie-Management-Systems für Lithium-Polymer Akkumulatoren. Bachelor's theses, FH Wedel, February, 2012

Ralf Weber

Untersuchung neuartiger Ceria-Nanopartikel für den Einsatz als Abrasiva beim chemisch-mechanischen Polieren (CMP). Diploma theses, Humboldt-Universität Berlin, August, 2012





PATENTS

Supplement 2011

W. Reinert

Verfahren zur Herstellung eines (Vielfach-) Bauelements auf Basis ultraplanner Metallstrukturen
DE 10 2007 060 785 B4

2012

T. Knieling

Mikromechanisches Element mit Temperaturstabilisierung
DE 10 2008 013 098 B4

K. Kohlmann-von Platen, D. Friedrich, H. Bernt

Halbleiterbauelement mit vertikalem Leistungsbau-element aufweisend einen Trenngraben und Verfahren zu dessen Herstellung
DE 103 00 577 B4

H.J. Quenzer, B. Wenk, B. Wagner

Assembly of Variable Capacitance
JP 4933016

U. Hofmann, M. Oldsen

Micro-mirror actuator having encapsulation capability and method for the production thereof
US 8,169,678 B2

M. Oldsen, U. Hofmann

Housing for micro-mechanical and micro-optical components used in mobile applications
US 8,201,452 B2

P. Merz, W. Reinert, M. Oldsen, O. Schwarzelbach

Micromechanical housing comprising at least two cavities having different internal pressure and/or different gas compositions and method for the production thereof
KR 10-1120205

H.J. Quenzer, G. Zwicker

Verfahren zur Oberflächenbehandlung einer elektrisch leitenden, metallischen Substratoberfläche
EP 2 010 351 B1

W. Reinert, P. Merz, D. Kähler

Leak test for a vacuum encapsulated device
IL 183 488

H. Futscher, G. Neumann

Method for producing drawn coated metals and use of said metals in the form of a current differentiator for electrochemical components
CA 2507399 C
JP 4996053

P. Birke, F. Birke-Salam

Films for electrochemical components and a method for production thereof
CA 2392702

U. Hofmann, M. Oldsen, B. Wagner

Electrostatic comb-drive micromechanical actuator
US 8,213,066 B2

U. Hofmann, M. Oldsen, B. Wagner

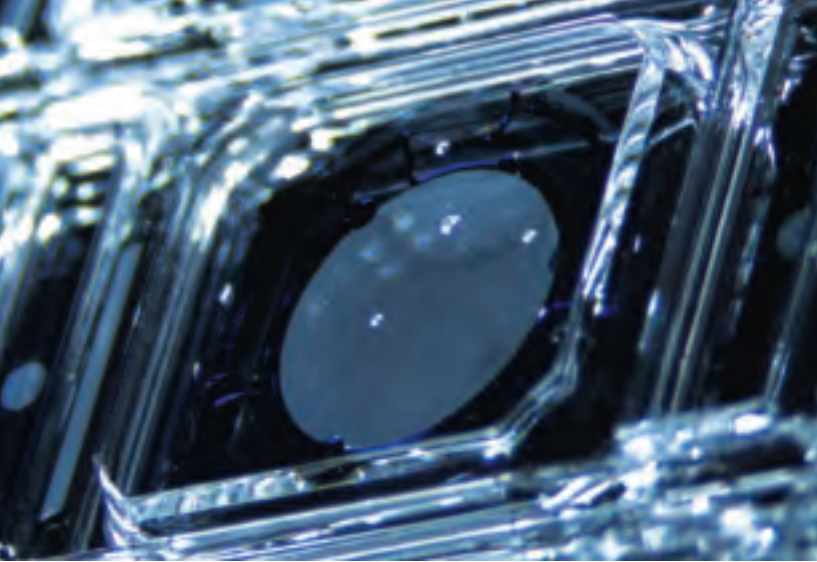
Mikromechanischer Aktuator mit elektrostatischem Kamm-Antrieb
DE 10 2008 059 634 B4

H.-J. Quenzer, G. Zwicker

Method for treating the surface of an electrically conducting substrate surface
JP 5140661

N. Marengo

Semiconductor arrangement with trench capacitor and method for production thereof
US 8,330,247 B2



OVERVIEW OF PROJECTS

- Ultrakompakte Leistungs-module höchster Zuverlässigkeit ULTIMO
- Simulationsstudie für Fast Recovery Dioden
- Energie-Effiziente Elektrische Antriebstechnik: Neue Umrichterkonzepte
- Lochmembranen im sub-0,5µm Bereich
- Super Junction PowerMOS
- Ultrathin Trench IGBTs on sub-100 µm Si-Substrates
- Entwicklung von poly-Si CMP Prozessen für die MEMS Herstellung Energy-Efficient Piezo-MEMS Tunable RF Front-End Antenna Systems for Mobile Devices (EPAMO)
- 9 D Sense; Development of Magnetic Field Sensors
- Untersuchung an mikromechanischen Drehraten-Sensoren
- Entwicklung von kapazitiven HF-Schaltern
- Entwicklung von piezoelektrischen Schichten für Si-Mikroaktuatoren
- Herstellung mikrooptischer Linsenarrays aus Glas
- Mikrolinsen aus Borosilikat-Glas
- High Volume Piezoelectric Thin Film Production Process for Microsystems, Piezo Volume
- Entwicklung von PZT-Schichten
- Mikroscan-Systeme für Display Anwendungen
- Herstellung mikrotechnischer analoger Ablenkeinheiten
- Magnetoelektronische Sensoren (Sonderforschungsbereich 855 der Uni Kiel)
- Entwicklung von LIDAR Systemen, MiniFaros
- Development and Fabrication of 256k CMOS Blanking Chips for Maskless Lithography
- Development of an ASIC for the control of BLDC-motors
- Dünnschicht Transducer PIETRA
- Siliziumbasierte Hochtemperatur-Thermogeneratoren auf 8" Wafer-Level (SIEGEN)
- Parallele Vermessung von mikromechanischen Inertialsensoren auf Waferebene
- Prozessentwicklung MEMS basierter Energie-Harvester
- Herstellung eines Multi Deflection Arrays für die hochauflösende Elektronenstrahl-Lithographie
- Entwicklung einer Montageplattform für Lasermodule und passive Optiken
- Entwicklung und Herstellung eines MEMS basierten hochgenauen CO₂-Sensors
- 3D-Signage
- TMC562 von und mit Trinamic
- Zellfreie Bioproduktion
- AOI Kalibriernormal (ZIM)
- Elektronischer Laktat Nachweis ELaN
- Zuverlässige Kontaktierung von Höchstleistungsbaulementen in der Leistungselektronik durch innovative Bändchen- und Litzenverbindungen (MAXIKON)
- Produktionsgerechtes reaktives Nanofügen zum hermetischen Versiegeln von Mikrosensoren auf Waferebene (REMTEC)

- *Glassfritt Vacuum Wafer Bonding*
- *Glaslotbonden mit strukturierten Capwafern und Musterwafern*
- *Wafer Level Packaging*
- *Process Development for Hermetic AuSn Vacuum Sealing of IR Sensors on Wafer Level*
- *Wafer Level Balling for 100 µm up to 500 µm Spheres*
- *Neon Ultra Fine Leak Test for Resonant Micro Sensors*
- *Solder Flip Chip on Flex*
- *Prozessoptimierung beim Selektivlöten für Anwendungen in der Leistungselektronik*
- *Zuverlässige Ag-sinterkontaktierte Halbleiterbauelemente für die regenerative Energietechnik (ZuSi)*
- *UV-Detektoren AlGaN (AGNES)*
- *Hochzuverlässige Stromrichter für Windenergieanlagen (HiReS)*
- *Tiefsee-Inspektions- und Explorations Technologie (TIETeK)*
- *Qualitätsbewertung an bleifreien Baugruppen*
- *Printed Electronics (Binäruhr, neuer Drucker LP50)*
- *Einfluss des Lotpastendrucks auf die Zuverlässigkeit der Lötstellen kritischer keramischer SMD-Komponenten auf FR4-Leiterplatten*
- *Jet-Dispensen*
- *Neue Analytik Computertomografie, 2D-Radiografie, Laserprofilometrie*
- *Ionische Liquide für elektrochemische Applikationen (IL-Echem)*
- *Flottenversuch Elektromobilität*
- *Hochenergie-Lithiumbatterien für die Zukunft-HE-LION*
- *Hochleistungslithiumbatterien mit Nanopartikeln in Core-Shell-Technologie LINACOR*
- *Entwicklung einer Zelltechnologie für Solarstrom-Zwischenspeicherung*
- *European Li-Ion Battery Manufacturing for Electric Vehicles (ELIBAMA)*

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Maïke Dudde: pages 6, 7, 8, 9 right, 90, 91

Fraunhofer-Gesellschaft, München: page 9 left

Fraunhofer IBMT, St. Ingbert: page 82

*Photo Company, Itzehoe: pages 4/5, 12, 14, 15, 16,
17 left, 18, 19, 21, 23, 30/31, 54/55, 59 left, 65, 66,
68, 69, 71 top, 73 right, 80, 95, 99, 100*

All other pictures Fraunhofer ISIT

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