Fraunhofer ISIT

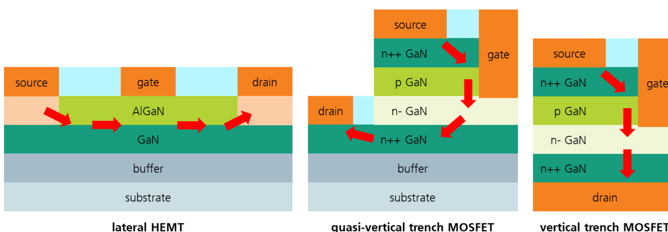
GaN technologies at Fraunhofer ISIT

Process capabilities, GaN innovations & our GaN roadmap

Process calibration test structures on a 8" GaN-on-Si wafer.

Under the motto "*From Planar to Vertical: Custom Solutions for Advanced Si- and GaN-based Power Electronics*" the Fraunhofer ISIT supports the continuous miniaturization of power electronic applications while increasing power density on system and device level. We have a proven background in application specific Si-based PowerMOS transistors, IGBTs and diodes with blocking capabilities up to 1200V. In 2017 we introduced the first GaN processes and equipment at Fraunhofer ISIT and started to develop advanced GaN transistors and diodes with excellent electrical properties and switching speeds down to the ns range.

For the manufacturing of these we are utilizing our 1000 m² GaN & MEMS fab in Itzehoe, Germany, that offers a unique combination of process capabilities and materials to unveil the potential of your GaN designs. Starting point are most commonly commercial and academic 8" GaN-on-Si and GaN-on-QST substrates with customizable epitaxies based on your device requirements.



Exemplary GaN device structures with increasing processing complexity.

Fraunhofer Institute for Silicon Technology ISIT

Dr. Michael Mensing
Head of the Advanced Devices Group
Business Unit Power Electronics

t: +49 4821 17 4331
michael.mensing@isit.fraunhofer.de

Fraunhoferstrasse 1
25524 Itzehoe, Germany
www.isit.fraunhofer.de

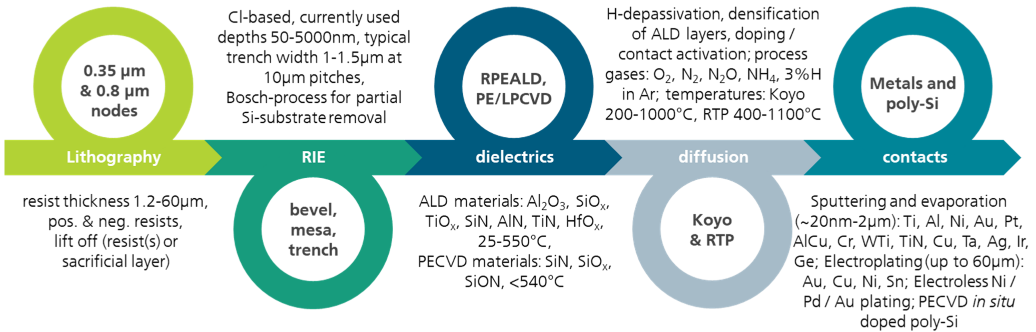
Check out our virtual fab tour:
s.fhg.de/isit360

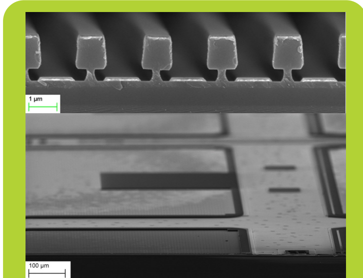
We are hiring!

PhD candidates, Postdocs and GaN specialists. Get in touch!

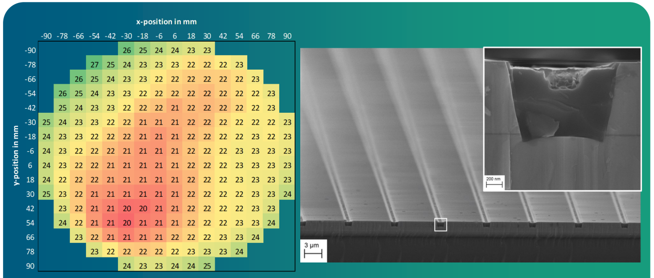
Process capabilities & innovations

Impression of the lithography area in ISIT's GaN & MEMS clean room.

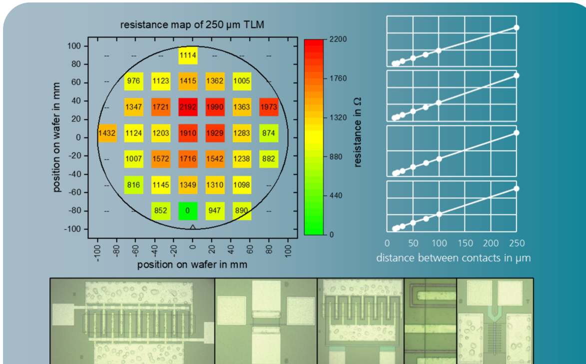




Advanced lift-off structures (top) and GaN -MOSFET metallization overview (bottom).



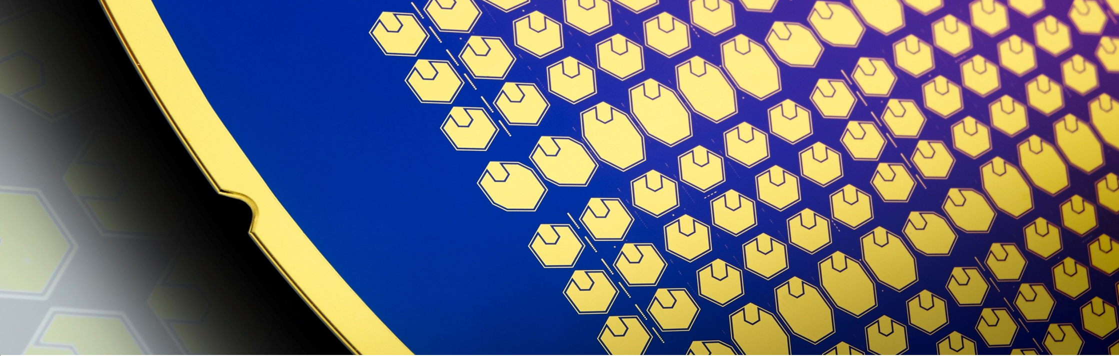
Left: Thermal-ALD SiO_2 thickness map in nm. Right: Trench etch and filling with an ALD-Al_2O_3 and subsequent PECVD in situ doped poly-Si.



AlGaN/GaN-HEMT 2deg-resistance wafer map, exemplary TLM-measurements and microscopy impressions of processed metallizations.

And more in development!

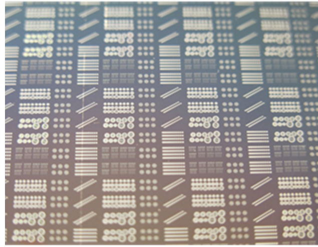
Peaked your interest? Get in touch with your possible challenges and let us solve them together.

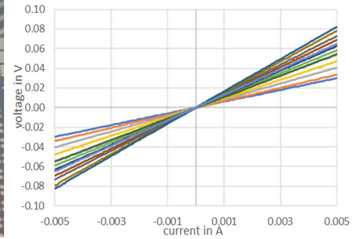


8″ quasi-vertical GaN diode wafer based on GaN-on-Si.

Metal-free ohmic GaN contact

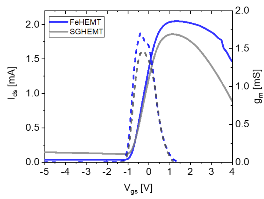
High quality ohmic contacts for GaN, that do not rely on noble metal alloys, are of great importance to maintain the efficiency throughout the entire lifecycle of the resulting devices. As such, the successful realization of an *in situ* doped poly-Si GaN-contact with unoptimized R_c~10^{-4} Ωcm² is a mayor step towards the CMOS compatibility and sustainability of GaN device manufacturing. The activation process utilizes a wafer-level laser-induced diffusion process that limits the thermal budget to the surface.

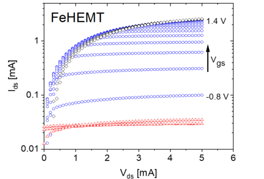




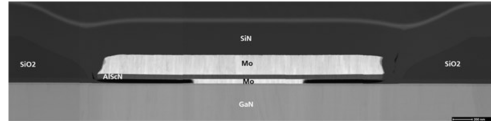
Processed GaN-on-Si wafer with in situ doped poly-Si contacts (left) and contact resistance measurements (right).

Integration of ferroelectric materials





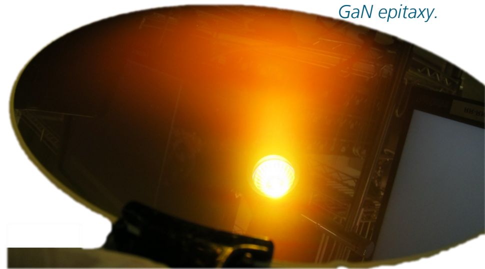
AlScN is the first nitride-based ferroelectric, discovered at Fraunhofer ISIT. Its composition is an ideal fit for GaN-based electronics. As such, we are exploring ways to augment transistor -properties by its integration, e.g. into the gate stack. In early prototypes we observed significant gm and on/off-ratio increases in comparison to Schottky-gate HEMTs. In the next step, we are seeking to create a switchable d-/e-mode device utilizing the programmable ferroelectric polarization, that can also function as a GaN-based memory.



Transfer characteristics of FeHEMT & SGHEMT and FeHEMT output characteristic (left).
TEM cross section of a AlScN-based FeHEMT gate with Mo contacts (right).

Next generation substrate technologies for high-power GaN devices

The unavailability of high breakdown voltages and power densities is one of GaN's challenges for automotive and industrial applications. Recently, e.g. Qromis substrate technology (QST) enabled the growth of thick GaN layers on the thermally matched substrate of poly-AlN. The material has been successfully introduced at ISIT. Look out for our next prototype releases!



QST-wafer with GaN epitaxy.

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Fraunhofer ISIT's facilities at the heart of Schleswig-Holstein.

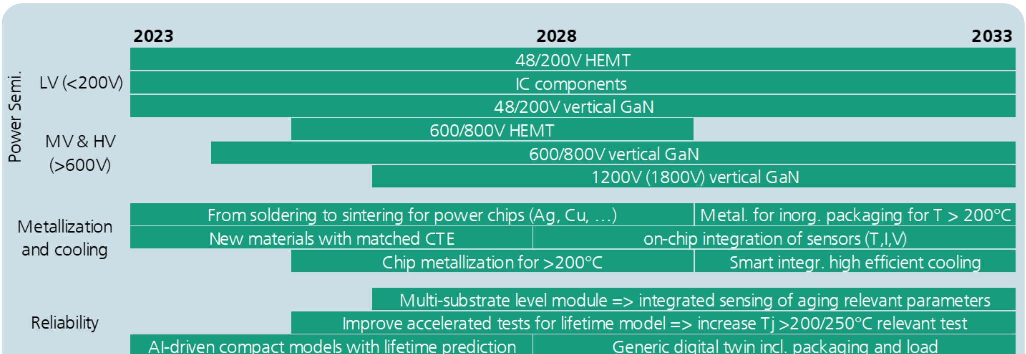
GaN technology roadmap at Fraunhofer ISIT

Feel free to join our collaboration network and let us help you shape your GaN R&D activities.

Fraunhofer ISIT has realized process blocks and device structures for HEMTs and quasi-vertical GaN devices. Based on novel substrate technologies and application demand for high-voltage GaN devices, we are developing fully vertical device structures on different 8" substrates.

Novel process blocks for these device structures include high quality gate dielectrics, precise GaN etch processes and improved metallization schemes. Additionally, high power densities and a demand for low-inductances are posing a challenge towards the integration and packaging approaches of these devices. Thus, we are already taking into account future metallization requirements and the codesign of novel cooling approaches for power devices on wafer level as well as by additive manufacturing techniques. Next, with increasing maturity of GaN implant and activation processes, more advanced vertical device concepts are taking shape.

Finally, the peculiarities of current and especially next gen. GaN devices are far from understood. To enhance and predict their reliability, we are including AI-methods in e.g. advanced behavior models, which will be an essential part of system level digital twin technologies on the rise.



High-level GaN technology development roadmap at Fraunhofer ISIT. Do you miss your topic? Get in touch!