Novel Integrated BEOL Compatible Inductances for Power Converter Applications

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***Abstract*—This paper presents the development, processing and investigation of micro-inductances on silicon having an inductance of about $150\,\mathrm{nH}$ and a resistance of $0.66\,\Omega$. The core of the inductances, $1\,\mathrm{mm}$ x $3.4\,\mathrm{mm}$ x $0.6\,\mathrm{mm}$ in size, is fabricated on silicon substrates using a novel fully back-end-of-line (BEOL) compatible fabrication technique based on the agglomeration of micro-sized magnetic powder by atomic layer deposition (ALD). In this way, a wide range of magnetic materials can be integrated on silicon substrates with a high degree of freedom regarding the dimensions of the core. That enables a lot of possibilities for innovative inductor designs for integrated power supplies. A typical boost converter with a GaN FET was designed to prove the functionality of micro-inductances based on such cores at a switching frequency of $20\,\mathrm{MHz}$. An input voltage of $15\,\mathrm{V}$ is boosted to $25\,\mathrm{V}$ on the output while a load current of $481\,\mathrm{mA}$ is applied. In this case the converter reaches an efficiency of $87\,\%$.**

I. Introduction

The miniaturization of passive components becomes more and more important to reach higher power densities in power supplies. At the same time applications like IoT, smartphones, smart homes, etc. require power converters with reduced size. This future trend is supported by wide band gap devices like SiC or GaN FETs, enabling a new level regarding power losses and switching frequencies. Due to switching frequencies in the range of 10-50 MHz, inductances for typical dc-dc converters become smaller than $200\,\mathrm{nH}$ [1], [2]. Therefore, MEMS fabrication technologies come into play for inductor designs [3]. The vision of a power supply in a package (PwrSiP) [4] and a power supply on a chip (PwrSoC) [5] becomes concrete by integrating inductors on silicon. The integration of inductors on silicon is investigated in several geometries with magnetic cores in [4], [6]–[10]. Commonly in-plane windings are utilized, for example spiral inductors [11]. The comparison between magnetic-core and air-core inductors in [12] yielded, that magnetic-core inductors have a better performance for applications up to $50\,\mathrm{MHz}$. However, air-core inductors perform better at higher frequencies due to eddy current losses in the magnetic core. In [13]–[16], approaches for 3D air-core inductors based on through-silicon vias (TSV) are developed. These air-core solutions need more space, thus their inductance density is quite low but future trends go to smaller and more efficient packages. Therefore, the combination of 3D TSV-based inductors with a magnetic core could be an interesting solution. Especially for a power supply in a package solution, it could be possible to fabricate the inductor and transistor on the same substrate, which would lead to low parasitics and a proper thermal management.

This paper presents a novel type of cores fabricated from micron-sized, soft magnetic powder using the powder agglomeration technique described in [17]. Since all particles in the core are surrounded by a dielectric layer and the points of contact between them are very small, eddy currents are suppressed and good characteristics are obtained even at high frequencies. In contrast to polymer-bonded cores, no degradation occurs at high temperatures or increased humidity. Magnetic powders of different materials with different particle size provided by several suppliers as well as mixtures of them were investigated regarding their electromagnetic behavior and compatibility with the fabrication process [18], [19]. Measurements on a vibrating sample magnetometer (VSM) and on an impedance analyzer show big differences between the investigated powders. To obtain inductors, these magnetic cores were hand-wound with wires around $100\,\mu\mathrm{m}$ diameter. The differences regarding their parameters and application range will be discussed in the following pages.

Finite-element-method (FEM) simulations were performed to validate the obtained results. Finally, as a proof-of-concept, a boost converter with a GaN FET and a switching frequency of $20\,\mathrm{MHz}$ was realized and tested using the novel inductors. Furthermore, this prototype should act as a flexible platform to investigate different inductor solutions and makes their comparison accessible. Accurate measurement equipment is used to analyze the electric and thermal behavior. In the next step, inductors based on the new core material shall be fabricated with TSVs instead of hand-wound wires while an optimized design is planned. Nevertheless, the existing sample was also used to calibrate a FEM model, based on that the design and optimization process is started for the next version.

The paper is organized as follows. Section 2 introduces briefly the fabrication process of silicon pieces with magnetic core. The samples are investigated regarding their electric characteristics up to $100\,\mathrm{MHz}$ in section 3. In addition, a pareto analysis points out which inductances are relevant for the application. In section 4, the use of FEM simulations is described while the measurements of section 3 are validated by simulation results. In section 5, a boost converter is designed and the development of the prototype is described. The electrical and thermal measurement results of this prototype are presented in section 6.

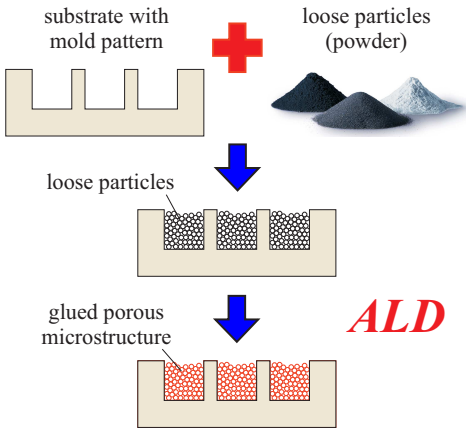


Fig. 1: Magnetic core fabrication process

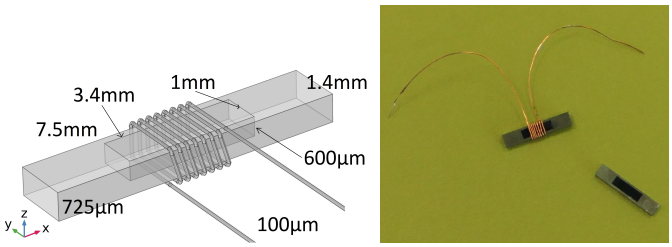


Fig. 2: Test samples

II. Fabrication Process of Magnetic Cores

The fabrication process is illustrated schematically in Fig. 1. First, a pattern of 3400 µm long, 1000 µm wide and 600 µm deep cavities is transferred by deep reactive ion etching (DRIE) into an 8 inch silicon substrate. After resist removal and cleaning, the substrate is diced into pieces, about 40 mm x 40 mm in size. In the next step, on each piece the cavities are manually filled with micron-sized magnetic particles of a particular type using doctor blade method. As magnetic materials carbonyl iron powder, alloy powder (QFeSi6.5) and MnZnP ferrite with the particle sizes between 1 to 100 µm were tested. Now, ALD is applied to agglomerate the initially loose particles within the cavities by a thin Al2O3 layer to rigid porous structures over the whole cavity depth [20]. By another dicing step, silicon chips as shown in Fig. 2 on the right are cut from each piece. To obtain inductors from those chips, 8 turns of 100 µm copper wire are manually wound around the central part with the embedded soft-magnetic core (Fig. 2). Finally, the wire is fixed with instant adhesive.

The powder-based MEMS technique illustrated in Fig. 1 is not limited to simple devices as fabricated within this work. It has already been shown that substrates with embedded porous 3D structures are fully back-end-of-line compatible and can be post-processed in a cleanroom environment. For example, in [21] a piezoelectric vibrational harvester with integrated NdFeB micro magnet array at the movable cantilever tip is presented. After integration of the micro magnets, three more mask layers as well as PECVD and various dry etching processes are needed to finalize the device. Suitable conditioning procedures to regain the cleanroom compatibility of substrates with embedded porous 3D structures are described in [22]. Besides the reproducibility of NdFeB-based porous 3D structures as well as their variation over a wafer is discussed. Similar values can be assumed for the soft-magnetic cores of the present work. After successful proof of the novel core material using simple hand-wound inductors more sophisticated devices with optimized core and integrated windings will be designed and fabricated.

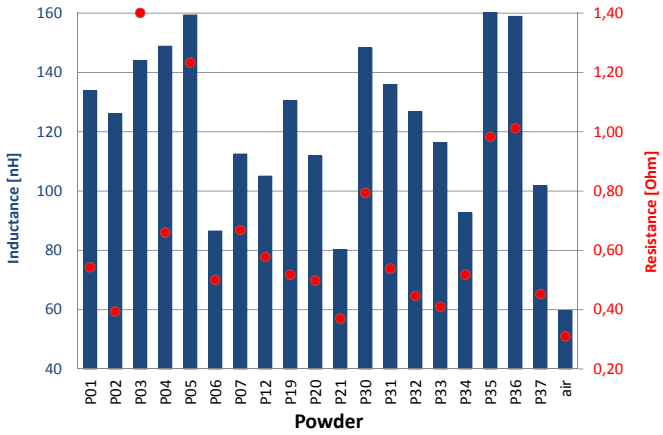


Fig. 3: Results of investigated powder-based cores at 20 MHz

III. Characterization of Inductors

Design parameters for an inductor are the number of turns N, area of the core A_{eff}, length of the core l_{eff} and the permeability μ_r. To estimate the inductance of a magnetic-core inductor (1) is widely used

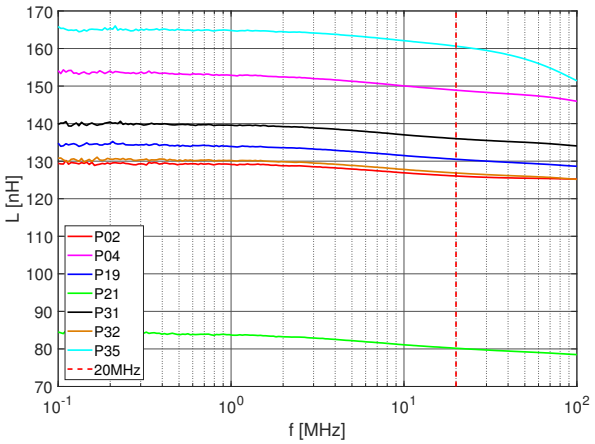
$$L = \frac{\mu_0 \mu_r A_{eff} N^2}{l_{eff}}. \quad (1)$$

As mentioned in [23], this classical model significantly overestimates the inductance enhancement in practical integrated inductors because of the demagnetization field inside the magnetic core; therefore, the calculation was adopted to

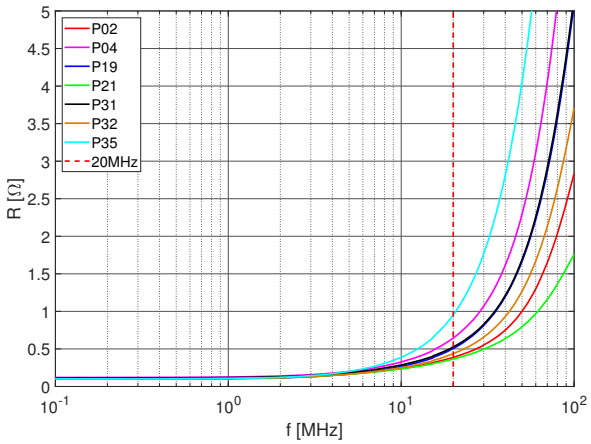
$$L = L_{air-core} + \Delta L \ , \ \Delta L = \frac{\mu_0 \mu_r A_{eff} N^2}{l_{eff}[1 + N_d(\mu_r - 1)]}, \quad (2)$$

where N_d is the demagnetization factor, which is about $1/7.8$ for this geometry. Assuming a permeability of 7, the inductance is about 138 nH based on (2). Adding about 10 nH for the wires at both ends of the inductor, the calculation comes close to the measurement results and FEM simulations provided in the next parts. Nevertheless, it is a rough estimation in which the distance between each winding and the diameter of the wire are neglected, therefore the FEM software is in use for future optimizations.

All 19 fabricated test samples were electrically characterized from 100 kHz to 100 MHz using a precision impedance analyzer (Agilent 4294A). At 20 MHz, the inductance is in



(a)



(b)

Fig. 4: Measurement results from impedance analyzer (from 100 kHz to 100 MHz): inductance (a) and resistance (b)

the range between 80 nH and 161 nH while the resistance is between 0.38 Ω and 1.4 Ω. As a reference, a sample without any magnetic powder in its cavity was measured, resulting in 60 nH and 0.31 Ω at 20 MHz. Fig. 3 gives an overview about the inductance and resistance of each test sample at 20 MHz. In addition, a pareto analysis was done for a better evaluation of the powders' performance. The plot in Fig. 6 shows the resistance and inverse inductance on its axes. Due to the definition of pareto optimality, one sample dominates another if its better in either the resistance or inductance and not worse in the other [24]. Applying this algorithm to all 19 inductors, 7 are evaluated as pareto-optimal (marked with a red circle in Fig. 6). One of these 7 inductors should be used depending whether a small resistance or a high inductance is desired. The measurement results of these 7 best samples are displayed over the whole frequency range in Fig. 4. Up to 6 MHz the resistance of all samples is quite similar but in higher frequencies significant differences are recorded. The inductances are quite stable from 100 kHz to 100 MHz, only sample 35 tends to decrease faster above 20 MHz. Another indicator is the quality factor $Q = \frac{L}{R} 2\pi f$ which is plotted in Fig. 5 showing values between 21 and 42 for the pareto-optimal inductors at 20 MHz.

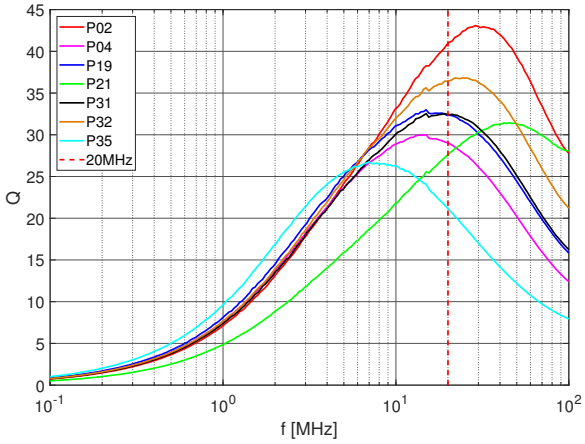


Fig. 5: Quality factor of pareto-optimal inductors

IV. Simulations

For the design of inductors a FEM software, in this case Comsol Multiphysics, is used with its magnetic fields (mf) physics for analysis in the frequency domain. In the first step, the geometry of the test sample was built as close as possible to reality. Especially the space between each winding has an important influence to the magnetic flux and to the results of the calculation for the inductance. Therefore, the geometry model was customized to the windings of the sample (Fig. 2). Once the geometry is set up, every component gets its proper material parameters. Comsol provides a library for typical materials like air, silicon, copper, etc. For the magnetic

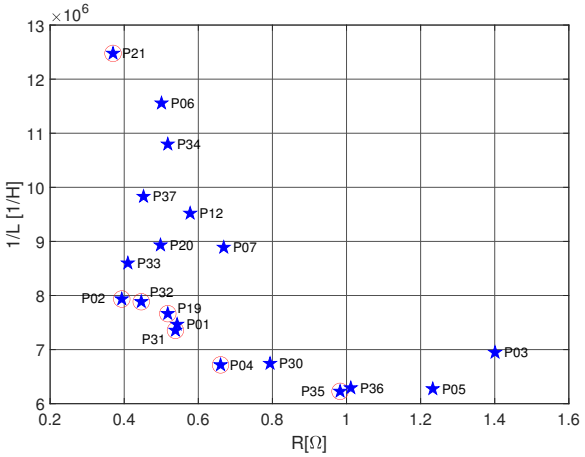


Fig. 6: Pareto analysis of 19 inductors at 20 MHz

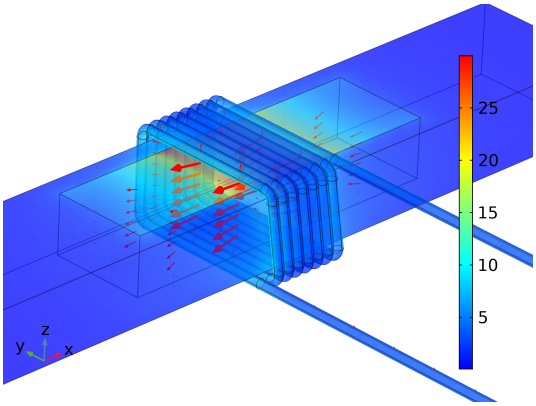


Fig. 7: FEM model, magnetic flux density (in mT) at 20 MHz

powder-based core, a few values had to be estimated by using the settings of alloy powder core ferrite and adjusting the permeability and electrical conductivity. As constraint, a sinusoidal current of 1A is supplied to one end of the wire while the other end is grounded. The frequency of this current source is set up for the range from 100 kHz to 100 MHz. After a simulation run, the complex impedance between both wire ends is known and the inductance can be calculated by dividing the imaginary part with its corresponding frequency while the resistance is just the real part. The impedance is given as

$$Z = R + j\omega L, \tag{3}$$

where

$$R = real\{Z\}, \qquad L = \frac{Im\{Z\}}{2\pi f}. \tag{4}$$

Measurements taken with the vibrating sample magnetometer (VSM) show a permeability of 7 for powder-based core 4; in addition the electrical conductivity was adopted to fit the curves of the impedance analyzer from 100 kHz to 100 MHz. As a result, the calculated inductance (148.80 nH) and resistance (668 mΩ) of the simulation is close to measured values ($L = 148.87$ nH and $R = 0.66\,\Omega$) at 20 MHz. These results confirm a proper reproduction of the magnetic core parameters in the FEM simulation whose visualization of the magnetic flux density is shown in Fig. 7. Based on this information, new geometries of the magnetic core are investigated and the design of the windings with TSVs is optimized depending on the fabrication possibilities.

V. Boost Converter Design

For testing the presented inductors, a dc-dc converter for voltages below 50 V and a power level of about 10-20 W was the goal for a first prototype. As topology, a standard boost converter was chosen (Fig. 8). The following calculations clarify that a switching frequency in MHz range is necessary for a boost converter with an inductor of 150 nH.

A. Converter design

The design is based on the inductor with powder-based core 4. As shown in Fig. 4a, this sample has an inductance of about

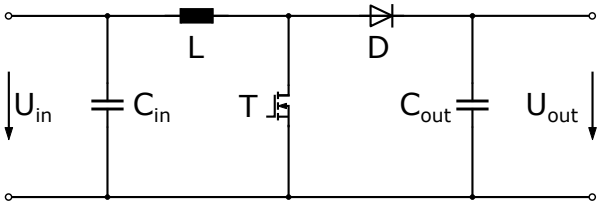


Fig. 8: Topology of boost converter

Parameter	Description	Value
U_{in}	Input voltage	15 V
D	Duty cycle	0.4
R	Load Resistance	50 Ω
f_{sw}	Switching frequency	20 MHz
L	Inductor	150 nH
R_L	Resistance of Inductor at 20 MHz	0.66 Ω

TABLE I: Design parameters of boost converter

150 nH. The input voltage is set to $U_{in} = 15$ V, while a duty cycle of $D = 0.4$ is applied. Therefore, the output voltage of an ideal boost converter in continuous conduction mode (CCM) is calculated as follows

$$\frac{U_{out}}{U_{in}} = \frac{1}{1-D}. \tag{5}$$

Rearranging (5) gives

$$U_{out} = U_{in}\frac{1}{1-D} = 15\,\text{V}\frac{1}{1-0.4} = 25\,\text{V}. \tag{6}$$

As load, a normal resistance is connected to the output terminals. In this case, $R = 50\Omega$ is chosen to burn

$$P_{out} = \frac{U_{out}^2}{R} = \frac{(25\,\text{V})^2}{50\,\Omega} = 12.5\,\text{W}. \tag{7}$$

For a converter in these power and frequency ranges, a reasonable efficiency of 70-80 % is common in literature (assuming an efficiency of $\eta = 0.80$ for next steps). Thus the input current I_{in} and averaged inductor current I_L are given by

$$I_L = I_{in} = \frac{I_{out}}{(1-D)\eta} = \frac{0.5\,\text{A}}{(1-0.4)\cdot 0.8} \approx 1.0\,\text{A}. \tag{8}$$

Working in CCM allows an inductor current ripple of 2 A and less, this results in a switching frequency of $f_{sw} \geq 20$ MHz. The inductor current ripple is given by

$$\Delta i_L = \frac{U_{in}D}{f_{sw}L}. \tag{9}$$

Rearranging (9) gives

$$f_{sw} \geq \frac{U_{in}D}{\Delta i_L L} = \frac{15\,\text{V}\cdot 0.4}{2\,\text{A}\cdot 150\,\text{nH}} = 20\,\text{MHz}. \tag{10}$$

In Table I, the parameters are listed, which are applied to the prototype and lead to the results being discussed in the next part.

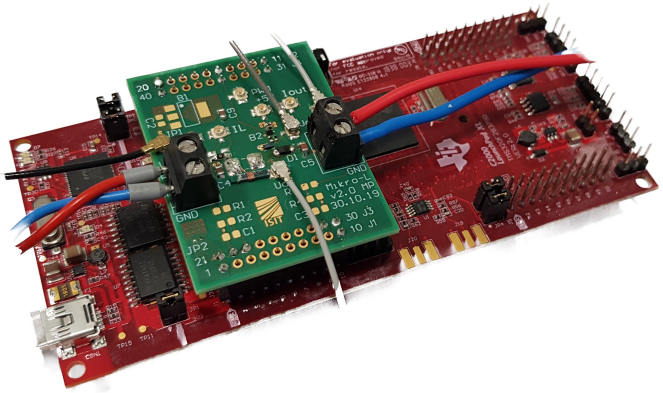


Fig. 9: Prototype with inductor sample 4

Symbol	Description
T	GaN FET (EPC8009, max. 65 V, 4 A)
D	Schottky diode (DB2W40200L, max. 40 V, 2 A)
C_{in}	Input capacitor (10 µF)
C_{out}	Output capacitor (100 nF)
L	Inductor (Powder-based core 4, 150 nH and 0.66 Ω at 20 MHz)
	Low-side GaN driver (LMG1020, max. 60 MHz)
	C2000 LaunchPadXL from Texas Instruments

TABLE II: Components of prototype

B. Prototype development

The boost converter was developed on a 40 mm x 52 mm PCB with 4 layers sitting piggyback on TI's LaunchpadXL (Fig. 9) whose microcontroller with a high resolution PWM up to 50 MHz could be easily programmed in C. It is realized as an open loop control at which the PWM signal can be adjusted in the code; nevertheless, two AD converters are connected to the input and output voltage, allowing closed loop control in the future. During the PCB development the focus was on a proper design to minimize the parasitic inductances, using the fast switching GaN FET at safe operation. The input voltage is applied to the terminals on the left side and on the terminal of the other side a 50 Ω resistor on a heatsink is connected. An EPC8009 GaN FET is used and can be switched up to 50 MHz in this setup, while the inductor sample with powder-based core 4 is used with $L = 150$ nH. The LMG1020 low-side GaN driver is used with gate resistors of 27 Ω and is supplied with +5 V from the LaunchPad. In Table II, the components of the prototype are listed.

VI. Experimental results and discussion

The measurements are recorded with the HDO4104 oscilloscope of LeCroy (2.5 GS/s), while passive probes are connected via coax cables to the U.FL sockets on the PCB. Based on the parameters of Table I, the measurement results are shown in Fig. 10. The gate voltage U_{gs} (red curve) changes between 0 V and 5 V every 50 ns with a duty cycle of $D = 0.4$, respectively the turn-on time is 20 ns. The input voltage U_{in}

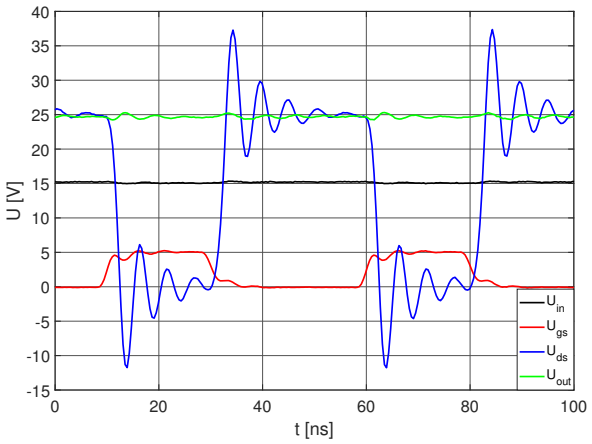


Fig. 10: Measurement results of boost converter

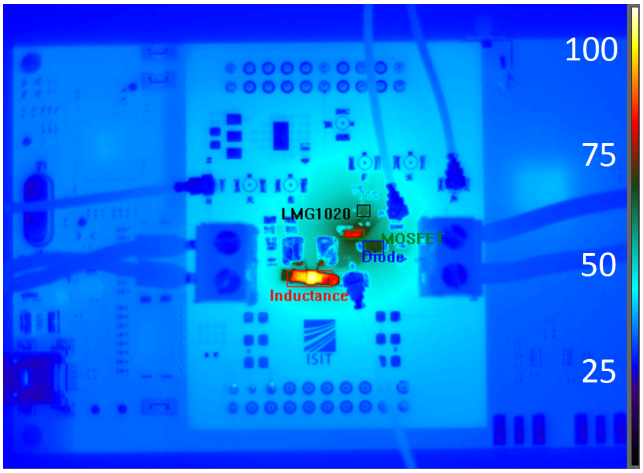


Fig. 11: Thermal image of converter with $U_{in} = 15$ V, $U_{out} = 25$ V and $P_{out} = 12$ W captured with FLIR A655SC camera

Component	Max. temperature
Inductor	108 °C
GaN FET	86 °C
Diode	69 °C
Driver IC	63 °C

TABLE III: Temperature measurements

(black curve) is measured with 15.1 V, whereas the output voltage U_{out} (green curve) is measured with 24.8 V. The blue curve shows the drain-source voltage across the GaN FET, because of the fast switching which comes along with GaN FET, even small parasitic inductances in the PCB layout conduct to a ringing effect. The voltage peak of 37 V is still in the safe operation area of this GaN FET. For calculation of the inverter's efficiency, the input $I_{in} = 0.91$ A and output current $I_{out} = 0.48$ A were measured with a current clamp for frequencies up to 100 MHz (CP031 from LeCroy).

The following calculation neglects the power consumption

of the gate driver IC, which is supplied from the LaunchPad. The efficiency is given by

$$\eta = \frac{P_{out}}{P_{in}} = \frac{U_{out} I_{out}}{U_{in} I_{in}} \approx \frac{11.90\,\mathrm{W}}{13.74\,\mathrm{W}} \approx 86.8\,\%. \qquad (11)$$

In Fig. 11 the image of the infrared camera shows where the power losses of $1.84\,\mathrm{W}$ are dissipated as thermal energy. The temperature of 4 main hot spots is identified and summed up in Table III.

VII. Conclusions and future work

In this paper a novel back-end-of-line compatible type of magnetic cores for integrated inductances is proposed, in which micron-sized powder were agglomerated by ALD. Based on a simple core geometry and manually wound windings with a $100\,\mu\mathrm{m}$ copper wire, 19 samples with cores obtained from different magnetic powders were characterized for switching frequencies from $100\,\mathrm{kHz}$ up to $100\,\mathrm{MHz}$. Detailed investigations at $20\,\mathrm{MHz}$ resulted in 7 pareto-optimal samples. FEM simulations show good agreement with the measurements and will be used for further designs. For practical testing of such inductors, a boost converter was designed and built. The proper operation of the converter prototype demonstrates the applicability of inductors with magnetic cores as fabricated by the novel powder-based MEMS technology. The efficiency calculation and thermal investigation correspond to the expectations.

Simulations are already in process for a new inductor design with TSVs; furthermore, thermal simulations show benefits because of a better thermal conductivity of silicon compared to commercial available inductors with wires.

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